EPSON
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S1V3S344
Hardware Specification

SEIKO EPSON CORPORATION

Rev. 1.1

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1. Outline

The S1V3S344 is an LSI with built-in flash memory and which offers pin compatibility with the existing S1V3034x Series.*1 The S1V3S344 is an LSI best suited to voice guidance products integrating the high quality decoding functions, a flash memory for voice data and a DA converter. Use of a speech data creation tool dedicated to the S1V3S344 enables the generation of high quality audio data with ease without the bother of studio recording. All the functions are controlled by commands over a serial interface and thus easily added onto any existing systems with a host processor.

Using the S1V3S344 allows prompt voice evaluation and reduces the time-to-market for products containing built-in voice guidance functions.

*1: The external components differ from those of S1V3034x Series.

2. Features

- Audio reproduction
  - High quality decoding (In EPSON's original format)
  - Bit rate: 40 kbps, 32 kbps, 24 kbps, 16 kbps
  - Sampling rate: 16 kHz
- Sequencer Messages
  - A sequence with up to 64 phrases can be set (no restriction on phrase combination)
  - Programmable delay time between phrases: 0 ms or 20 to 2047 ms (in 1-ms steps)
- Built-in flash memory for voice data
  - Includes the following flash memory capacity assigned to voice data.
    - 512 Kbytes (approx. 4 mins / 16 kbps)
    - Reliability
      - Erase/write cycles: 1,000 cycles (minimum), 10,000 cycles (Typ.)
      - Data retention: 10 years (minimum)
    - Flash memory access communication format (chip erasure, writing, reading)
      - Clock synchronous serial interface
- Host Interface
  - Clock synchronous serial interface
    - Asynchronous serial interface (UART)
      (Supported only when system clock is 32.768 kHz)
  - I2C interface
  - Command Control
- 16-bit DA converter
  - Sampling rate (f_s): 16 kHz
  - Input bit: 16 bits
  - System clock
    - Frequency (direct input): 32.768 kHz or 12.288 MHz
    - Frequency (oscillator): 32.768 kHz
- Package
  - 52-pin QFP (10 mm x 10 mm) with 0.65 mm pitch-pins
- Supply voltage
  - 4.5 V to 5.5 V (single power supply)
  - 3.0 V to 3.6 V (single power supply)

3. Pinout Diagram

3.1 QFP13-52

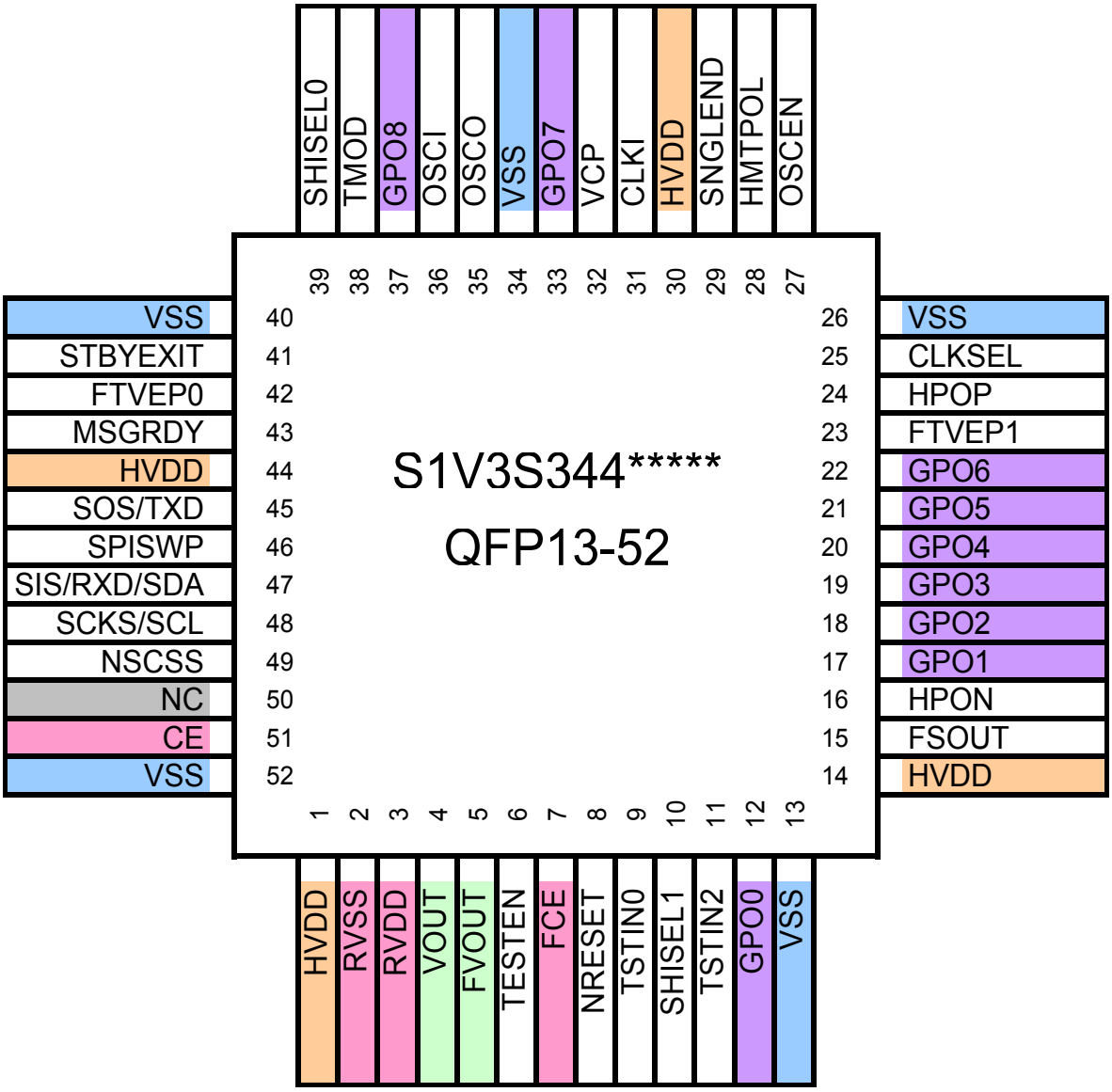


Figure 3.1 Pinout diagram (QFP13-52)

4. Pin Description

- Symbols

  I = Input pin

  O = Output pin

  IO = Bi-directional pin

  P = Power Pin

  Z = High Impedance

- I/O Cells

Symbol	Function
IC	LVCMOS Input
IH	LVCMOS Schmitt level Input
O1	Output Buffer (2.0 mA / -2.0 mA output current when 5.0 V (typ))
T1	3-state Output Buffer (2.0 mA / -2.0 mA output current when 5.0 V (typ))
T2	3-state Output Buffer (4.0 mA / -4.0 mA output current when 5.0 V (typ))
BC1	Bi-directional IO Buffer (2.0 mA / -2.0 mA output current when 5.0 V (typ))
LLIN	Transparent Input (1.8 V)
LLOT	Transparent Output (1.8 V)
HLIN	Transparent Input (HVDD)
ITST1	Test input with pull-down resistor (120 kΩ when 1.8 V (typ))
HZTST	Flash macro test input

Pin Name	Pin (52)	I/O	I/O Cell Type	State at NRESET=L	I/O Power	Function
Serial Interface						
SIS/RXD/SDA	47	IO	BC1	Z	HVDD	[Clock syncronous] Serial Data Input [Asynchronous] Serial Data Input [I2C] Data input/output
SCKS/SCL	48	I	IC	Z	HVDD	[Clock syncronous] Serial Clock Input [Asynchronous] H-level fixed [I2C] Serial Clock Input
SOS/TXD	45	O	T2	See section 5.3	HVDD	[Clock syncronous] Serial Data Output [Asynchronous] Serial Data Output [I2C] Open
NSCSS	49	I	IC	Z	HVDD	[Clock syncronous] Slave Device Select Input (L active) [Asynchronous] L fixed [I2C] L fixed
MSGRDY	43	O	O1	L	HVDD	Serial Output Data Ready (H active)
SHISEL0	39	I	IC	Z	HVDD	Serial interface selection SHISEL[1:0] = LL: Clock syncronous SHISEL[1:0] = *H: Asynchronous SHISEL[1:0] = HL: I2C
SHISEL1	10	I	IC	Z	HVDD	

Standby mode control						
STBYEXIT	41	I	IC	Z	HVDD	STANDBY mode exit control Input (L: Exit STANDBY mode, H: Continue STANDBY mode)
Audio output						
HPOP	24	O	T2	Z	HVDD	Audio output
HPON	16	O	T2	Z	HVDD	Audio output (Can be set so that output stops when SNGLEND = H (L level).)
System clock						
CLKI	31	I	IC	Z	HVDD	Clock input (See section 5.2)
OSCI	36	I	LLIN	Z	-	Oscillator connector pin (See section 5.2)
OSCO	35	O	LLOT	-	-	Oscillator connector pin (See section 5.2)
CLKSEL	25	I	IC	Z	HVDD	System clock frequency selection (L: 32.768 kHz, H: 12.288 MHz) (See section 5.2)
OSCEN	27	I	IC	Z	HVDD	System clock source selection (L: CLKI input, H: oscillator (OSCI/OSCO)) (See section 5.2)
Hardware reset						
NRESET	8	I	IH	Z	HVDD	Hardware reset input (L active)
Mode setting						
SNGLEND	29	I	IC	Z	HVDD	Audio output mode selection (L: differential output, H: single end output)
HMTPOL	28	I	IC	Z	HVDD	L fixed
Test input/output						
TESTEN	6	I	ITST1	Pull-down	-	Test pin (Connected to VSS during normal operations)
VCP	32	O	LLOT	-	-	Test pin (Open during normal operations)
TSTIN2	11	I	IC	Z	HVDD	Test pin (Connected to VSS during normal operations)
TSTIN0	9	I	IC	Z	HVDD	Test pin (Connected to VSS during normal operations)
FSOUT	15	O	T1	Z	HVDD	Test pin (Open during normal operations)
Built-in flash test pins						
TMOD	38	I	IC	Z	HVDD	Test pin (Connected to VSS with 1 kΩ during normal operations)
SPISWP	46	I	IC	Z	HVDD	Test pin (Connected to VSS during normal operations)
FTVEP1	23	I	HZTST	Z		Test pin (Connected to HVDD during normal operations)
FTVEP0	42	I	HZTST	Z		Test pin (Connected to HVDD during normal operations)

(Continues to the next page)

4. Pin Description

Internal voltage drop regulator						
CE	51	I	HLIN	Z	HVDD	Test pin (Connected to HVDD during normal operations)
FCE	7	I	HLIN	Z	HVDD	Test pin (Connected to HVDD during normal operations)
VOUT	4	O	-	-	-	Internal voltage drop regulator output pin (1.8 V) (Connect 1 µF capacitor between VOUT and RVSS.)
FVOUT	5	O	-	-	-	Internal voltage drop regulator output pin (3.3 V) (Connect 4.7 µF capacitor between VOUT and RVSS.)

Pin name	Pin (52)	I/O	Function
Power supply			
HVDD	1, 14, 30, 44	P	IO cell power supply
VSS	13, 26, 34, 40, 52	P	Internal area and IO cell GND
RVDD	3	P	Internal voltage drop regulator power supply
RVSS	2	P	Internal voltage drop regulator GND
General-purpose output pin			
GPO	12, 17, 18, 19, 20, 21, 22, 33, 37	O	General-purpose output pin (Open during normal operations)
Unused pins			
NC	50	NC	Unused pins

5. Function Description

5.1 Standard Application System

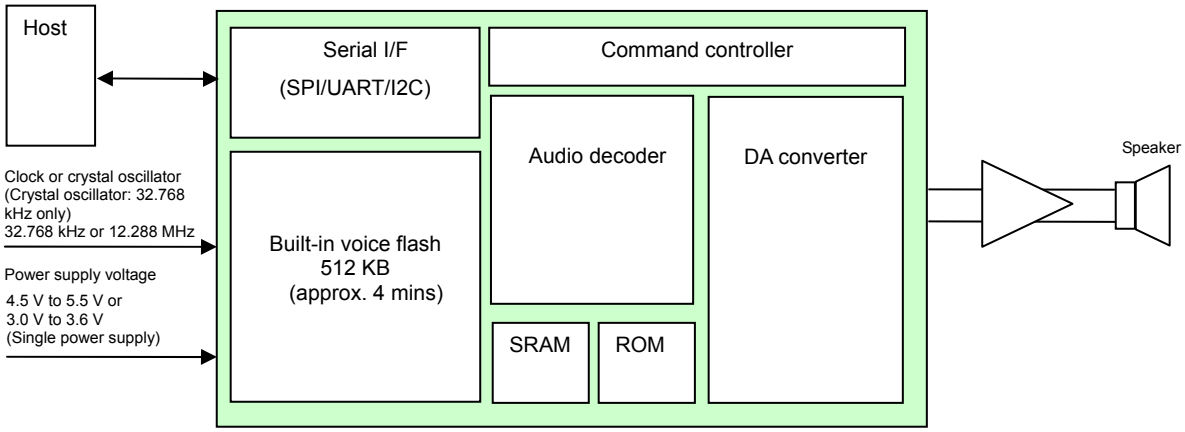


Figure 5.1 Standard application system

Figure 5.1 shows a standard S1V3S344 application system. The host controls the S1V3S344 with commands (message protocol) issued via the serial interface. After Power On Reset, the S1V3S344 outputs audio from the internal DA converter while internally decode-processing the compressed audio data from the internal audio data flash memory or issued from the host.

For details of commands, refer to *S1V3034x Series Message Protocol Specification* and *Flash Access Specifications*.

For more information on voice guidance creation tools, refer to *EPSON Speech IC Voice Guidance Creation Tool User Guide*.

5.2 System Clock

The S1V3S344 system clock frequency can be set to either 32.768 kHz or 12.288 MHz. The clock source can be set to be either direct input (input from CLKI pin) or oscillator (connected to OSCI/OSCO pin). The oscillator, however, can be used with 32.768 kHz only. The frequency and clock source settings are defined by the input pin CLKSEL and OSCEN settings. Table 5.1 shows system clock mode settings.

Table 5.1 System clock mode settings

Mode setting		Clock frequency	Clock pin settings		
CLKSEL	OSCEN		CLKI	OSCI	OSCO
0	0	32.768 kHz	32.768 kHz input	L level input	Open
0	1	32.768 kHz	L level input	Connect 32.768 kHz oscillator	
1	0	12.288 MHz	12.288 MHz input	L level input	Open
1	1	-	**Must not be selected**		

5.3 Serial Interface

The S1V3S344 serial interface can be set to clock synchronous, asynchronous (UART), or I2C.

However, only clock synchronous serial transfer can be used for directly accessing the flash memory. Direct access to the flash memory is not possible with UART or I2C formats.

- Clock synchronous

  Supports slave mode.

  Data length: 8-bit, fixed, MSB first

- Asynchronous (UART)

  Data length: 8-bit, fixed, LSB first

  Start bit: 1-bit, fixed

  Stop bit: 1-bit or 2-bit, selectable (default: 1-bit)

  Parity bit: Even, odd, or none, selectable (default: none)

  Baud rate [bps]: 460 k, 230 k, 115 k, 57.6 k, 38.4 k, 19.2 k, 9.6 k (default: 9.6 kbps)

- I2C

  Supports I2C slave mode.

  Maximum transfer speed: 83.3 kHz (when I2C bus rising time is 480 ns or less)

Serial interface selection is defined by the input pin SHISEL[1:0] settings.

Table 5.2 lists serial interface mode settings.

Table 5.2 Serial interface mode settings

SHISEL		Interface	Serial interface pin settings			
1	0		SCKS	SIS	SOS	NSCSS
0	0	Clock synchronous	Serial clock input	Data input	Data output	Slave selection input
0	1	UART	H-level input	Data input	Data output	L-level input
1	1					
1	0	I2C	Serial clock input	Data input/output	(Open)	L-level input

Table 5.3 shows the pin states when hardware resetting is enabled (NRESET=L).

Table 5.3 States when hardware resetting is enabled (serial interface)

SHISEL		Interface	States for NRESET=L (L: L-level output, H: H-level output, Z; High-impedance)			
1	0		SCKS	SIS	SOS	NSCSS
0	0	Clock synchronous	Z	Z	Dependent on NSCSS input level L (when NSCSS = L) Z (when NSCSS = H)	Z
0	1	UART	Z	Z	H	Z
1	1					
1	0	I2C	Z	Z	Z	Z

Note:

- **The asynchronous serial interface (UART) is not available when the selected system clock frequency is 12.288 MHz.**
- **The maximum transfer speed of the I2C interface is 83.3 kHz. This maximum transfer speed is based on the I2C bus rising time of 480 ns or less. It should be noted that the maximum transfer speed will be lower if the I2C bus rising time exceeds 480 ns due to the load capacity and pull-up resistance.**
- **When using the I2C interface, it is recommended to use the sequence playback.**

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6.1 Absolute maximum ratings

(VSS = 0 V)

Parameter	Symbol	Rate Value	Unit
Supply Voltage	HVDD	VSS-0.3 to 7.0	V
	RVDD	VSS-0.3 to 7.0	V
Input Voltage	HVI	VSS-0.3 to HVDD+0.5	V
Output Voltage	HVO	VSS-0.3 to HVDD+0.5	V
Output Current/Pin	IOUT	±10	mA
Storage Temperature	Tstg	-65 to +150	°C

6.2 Recommended Operating Conditions

(1) When using 5.0 V (typ) power supply

Table 6.2 Recommended operating conditions for 5 V power supply voltage

(VSS = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	HVDD	2.2	-	5.5	V
	RVDD	2.2	-	5.5	V
Input Voltage	HVI	VSS	-	HVDD	V
Output Voltage	HVO	VSS	-	HVDD	V
Ambient Temperature	Ta: Erase/ write	-40	-	70	°C
	Ta: Read	-40	-	85	°C

(2) When using 3.3 V (typ) power supply

Table 6.3 Recommended operating conditions for 3.3 V power supply voltage

(VSS = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	HVDD	3.0	-	3.6	V
	RVDD	3.0	-	3.6	V
Input Voltage	HVI	VSS	-	HVDD	V
Output Voltage	HVO	VSS	-	HVDD	V
Ambient Temperature	Ta: Erase/ write	-40	-	70	°C
	Ta: Read	-40	-	85	°C

6.3 DC Characteristics

6.3.1 DC Characteristics for 5.0 V ±0.5 V Power Supply Voltage

Table 6.4 DC characteristics for 5.0 V ±0.5 V power supply voltage

(HVDD / RVDD = 5.0 ±0.5 V, VSS = 0 V, Ta = -40°C to 85°C, erase/write Ta = -40°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage						
Supply current Erase/write	IFCEPGH	HVDD=5.5 V RVDD=5.5 V	-	0.2	-	mA
(unloaded)	IFCEPGR		-	24	-	mA
Supply current	IDDH		-	0.3	-	mA
(unloaded) *1	IDDR		-	4.2	-	mA
Static current						
Supply current *2	IDDSH	VIN=HVDD or VSS	-	0.3	-	μA
	IDDSR	HVDD=5.5 V RVDD=5.5 V	-	52	-	μA
Input leakage current						
Input leakage current		HVDD=5.5 V RVDD=5.5 V VIH=HVDD VIL=VSS	-5	-	5	μA
Input characteristics (LVCMOS)	Pin names: SIS, SCKS, NSCSS, SHISEL[1:0], STBYEXIT, CLKI, CLKSEL, SNGLEND, HMTPOL, OSCEN, TSTIN2, TSTIN0, SPISWP, TMOD					
H-level input voltage	VIH1	HVDD=5.5 V	3.5	-	-	V
L-level input voltage	VIL1	HVDD=4.5 V	-	-	1.0	V
Schmitt input characteristic (LVCMOS)	Pin names: NRESET					
H-level input voltage	VIH2	HVDD=5.5 V	2.0	-	4.0	V
L-level input voltage	VIL2	HVDD=4.5 V	0.8	-	3.1	V
Hysteresis voltage	ΔV	HVDD=4.5 V	0.3	-	-	V
Output characteristics	Pin names: SIS, MSGRDY, FSOUT, TSTOUT0, GPO0-GPO8					
H-level output voltage	VOH1	HVDD=4.5 V IOH=-2 mA	HVDD-0.4	-	-	V
L-level output voltage	VOL1	HVDD=4.5 V IOL=2 mA	-	-	VSS+0.4	V
Output characteristics	Pin names: SOS, HPOP, HPON					
H-level output voltage	VOH2	HVDD=4.5 V IOH=-4 mA	HVDD-0.4	-	-	V
L-level output voltage	VOL2	HVDD=4.5 V IOL=4 mA	-	-	VSS+0.4	V
Output characteristics	Pin names: SIS, SOS, HPOP, HPON, FSOUT, TSTOUT0					
Off-state leakage current	IOZ	-	-5	-	5	μA
Pin capacitance	Pin names: All input pins					
Input pin capacitance	CI	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF

Pin capacitance		Pin names: All output pins					
	Output pin capacitance	CO	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF
Pin capacitance		Pin names: All Bi-directional pins					
	Bi-directional pin capacitance	CIO	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF

*1: Approximately current values during decoding under the recommended operating conditions (Ta=25°C)
(Audio output has no load.)

*2: Static current under the recommended operating conditions (Ta=25°C)

6.3.2 DC Characteristics for 3.3 V ±0.3 V Power Supply Voltage (1)

Table 6.5 DC characteristics for 3.3 V ±0.3 V power supply voltage

(HVDD / RVDD = 3.3 ±0.3 V, VSS = 0 V, Ta = -40°C to 85°C, erase/write Ta = -40°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage						
Supply current Erase/write	IFCEPGH	HVDD=3.3V RVDD=3.3V	-	0.13	-	mA
(unloaded)	IFCEPGR		-	21	-	mA
Supply current	IDDH		-	0.2	-	mA
(unloaded) *1	IDDR		-	4.1	-	mA
Static current						
Supply current *2	IDDSH	VIN=HVDD or VSS HVDD=3.3V RVDD=3.3V	-	0.1	-	µA
	IDDSR		-	48	-	µA
Input leakage current						
Input leakage current		HVDD=3.6 V RVDD=3.6 V VIH=HVDD VIL=VSS	-5	-	5	µA
Input characteristics (LVCMOS)	Pin names: SIS, SCKS, NSCSS, SHISEL[1:0], STBYEXIT, CLKI, CLKSEL, SNGLEND, HMTPOL, OSCEN, TSTIN2, TSTIN0, SPISWP, TMOD					
H-level input voltage	VIH1	HVDD=3.6 V	2.2	-	-	V
L-level input voltage	VIL1	HVDD=3.0 V	-	-	0.8	V
Schmitt input characteristic (LVCMOS)	Pin names: NRESET					
H-level input voltage	VIH2	HVDD=3.6 V	1.2	-	2.52	V
L-level input voltage	VIL2	HVDD=3.0 V	0.75	-	1.98	V
Hysteresis voltage	ΔV	HVDD=3.0 V	0.3	-	-	V
Output characteristics	Pin names: SIS, MSGRDY, FSOUT, TSTOUT0, GPO0-GPO8					
H-level output voltage	VOH1	HVDD=3.0 V IOH=-1.4 mA	HVDD-0.4	-	-	V
L-level output voltage	VOL1	HVDD=3.0 V IOL=1.4 mA	-	-	VSS+0.4	V
Output characteristics	Pin names: SOS, HPOP, HPON					
H-level output voltage	VOH2	HVDD=3.0 V IOH=-2.8 mA	HVDD-0.4	-	-	V
L-level output voltage	VOL2	HVDD=3.0 V IOL=2.8 mA	-	-	VSS+0.4	V
Output characteristics	Pin names: SIS, SOS, HPOP, HPON, FSOUT, TSTOUT0					
Off-state leakage current	IOZ	-	-5	-	5	µA
Pin capacitance	Pin names: All input pins					
Input pin capacitance	CI	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF

Pin capacitance		Pin names: All output pins					
	Output pin capacitance	CO	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF
	Pin capacitance	Pin names: All Bi-directional pins					
	Bi-directional pin capacitance	CIO	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF

*1: Approximately current values during decoding under the recommended operating conditions (Ta=25°C)
(Audio output has no load.)

*2: Static current under the recommended operating conditions (Ta=25°C)

6.3.3 DC Characteristics for 3.3 V ±0.3 V Power Supply Voltage (2)

Table 6.6 DC characteristics for 3.3 V ±0.3 V power supply voltage

(HVDD / RVDD = 3.3 ±0.3 V, VSS = 0 V, Ta = -40°C to 85°C, erase/write Ta = -40°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage						
Supply current Erase/write	IFCEPGH	HVDD=3.0 V RVDD=3.0 V	-	0.12	-	mA
(unloaded)	IFCEPGR		-	16	-	mA
Supply current	IDDH		-	0.17	-	mA
(unloaded) *1	IDDR		-	4.0	-	mA
Static current						
Supply current *2	IDDSH	VIN=HVDD or VSS HVDD=3.0 V RVDD=3.0 V	-	0.1	-	µA
	IDDSR		-	45	-	µA
Input leakage current						
Input leakage current		HVDD=3.6 V RVDD=3.6 V VIH=HVDD VIL=VSS	-5	-	5	µA
Input characteristics (LVCMOS)	Pin names: SIS, SCKS, NSCSS, SHISEL[1:0], STBYEXIT, CLKI, CLKSEL, SNGLEND, HMTPOL, OSCEN, TSTIN2, TSTIN0, SPISWP, TMOD					
H-level input voltage	VIH1	HVDD=3.6 V	2.2	-	-	V
L-level input voltage	VIL1	HVDD=3.0 V	-	-	0.8	V
Schmitt input characteristic (LVCMOS)	Pin names: NRESET					
H-level input voltage	VIH2	HVDD=3.6 V	1.2	-	2.52	V
L-level input voltage	VIL2	HVDD=3.0 V	0.75	-	1.98	V
Hysteresis voltage	ΔV	HVDD=3.0 V	0.3	-	-	V
Output characteristics	Pin names: SIS, MSGRDY, FSOUT, TSTOUT0, GPO0-GPO8					
H-level output voltage	VOH1	HVDD=3.0 V IOH=-1.4 mA	HVDD-0.4	-	-	V
L-level output voltage	VOL1	HVDD=3.0 V IOL=1.4 mA	-	-	VSS+0.4	V
Output characteristics	Pin names: SOS, HPOP, HPON					
H-level output voltage	VOH2	HVDD=3.0 V IOH=-2.8 mA	HVDD-0.4	-	-	V
L-level output voltage	VOL2	HVDD=3.0 V IOL=2.8 mA	-	-	VSS+0.4	V
Output characteristics	Pin names: SIS, SOS, HPOP, HPON, FSOUT, TSTOUT0					
Off-state leakage current	IOZ	-	-5	-	5	µA
Pin capacitance	Pin names: All input pins					
Input pin capacitance	CI	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF

Pin capacitance		Pin names: All output pins					
	Output pin capacitance	CO	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF
Pin capacitance		Pin names: All Bi-directional pins					
	Bi-directional pin capacitance	CIO	f=1 MHz HVDD=RVDD=0 V	-	-	8	pF

*1: Approximately current values during decoding under the recommended operating conditions (Ta=25°C)
(Audio output has no load.)

*2: Static current under the recommended operating conditions (Ta=25°C)

6.4 AC Characteristics

6.4.1 System Clock Timing (32.768 kHz)

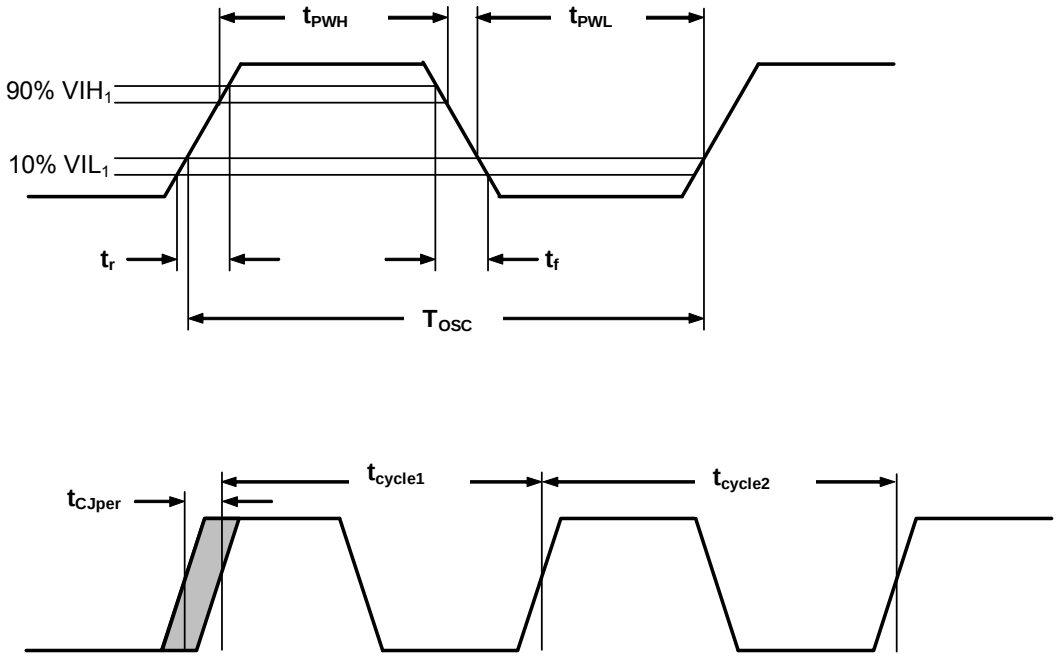


Figure 6.1 System clock timing (32.768 kHz)

Table 6.7 AC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{OSC}	Input clock frequency	-	32.768	-	kHz
T_{OSC}	Input clock period	-	1/fosc	-	ms
t_{pwh}	Input clock pulse width high	0.45*T_{osc}	-	0.55*T_{osc}	ms
t_{pwl}	Input clock pulse width low	0.45*T_{osc}	-	0.55*T_{osc}	ms
t_r	Input clock rising time (10% → 90%)	-	-	5.0	µs
t_f	Input clock falling time (90% → 10%)	-	-	5.0	µs
t_{CJper}	Input clock period jitter (*2, 4)	-5.0	-	5.0	ns
$t_{CJcycle}$	Input clock cycle jitter (*1, 3, 4)	-5.0	-	5.0	ns
*1	$t_{CJcycle} = t_{cycle1} - t_{cycle2}$				
*2	The input clock period jitter is the displacement relative to the center period (reciprocal of center frequency).				
*3	The input clock cycle jitter is difference in period between adjacent cycles.				
*4	The jitter characteristics must meet both t_{Cjper} and $t_{CJcycle}$ characteristics.				
*	Ensure that clock overshoot/undershoot does not exceed absolute maximum ratings in Table 6.1.				

6.4.2 System Clock Timing (12.288 MHz)

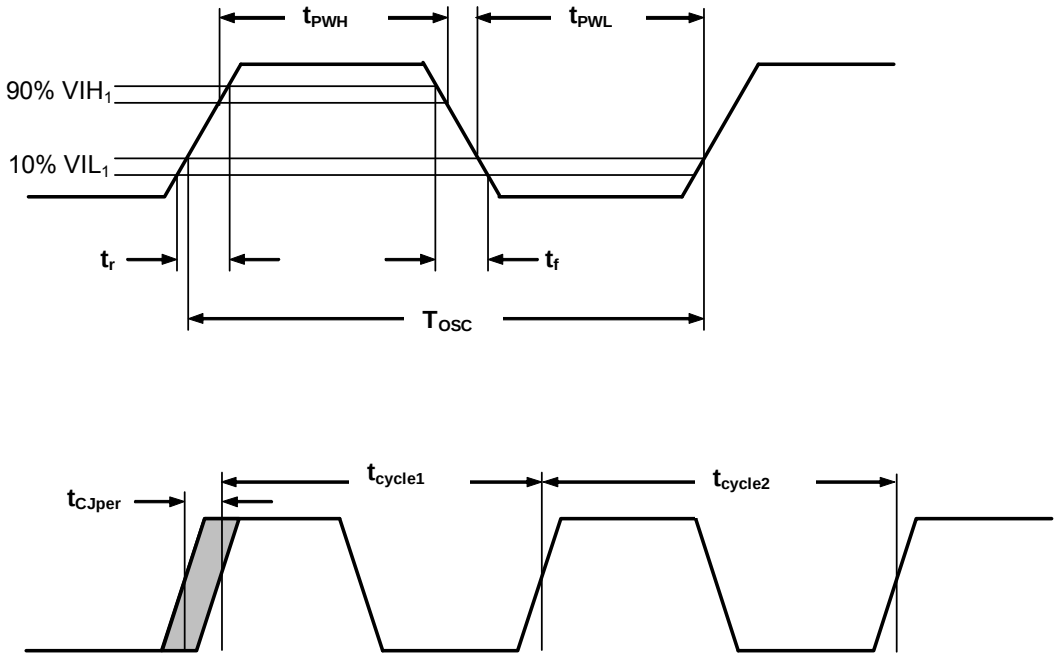


Figure 6.2 System clock timing (12.288 MHz)

Table 6.8 System clock timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{OSC}	Input clock frequency	-	12.288	-	MHz
T_{OSC}	Input clock period	-	1/fosc	-	µs
t_{pwh}	Input clock pulse width high	0.45*T_{osc}	-	0.55*T_{osc}	µs
t_{pwl}	Input clock pulse width low	0.45*T_{osc}	-	0.55*T_{osc}	µs
t_r	Input clock rising time (10% → 90%)	-	-	5.0	ns
t_f	Input clock falling time (90% → 10%)	-	-	5.0	ns
t_{CJper}	Input clock period jitter (*2, 4)	-400	-	400	ps
$t_{CJcycle}$	Input clock cycle jitter (*1, 3, 4)	-400	-	400	ps
*1	$t_{CJcycle} = t_{cycle1} - t_{cycle2}$				
*2	The input clock period jitter is the displacement relative to the center period (reciprocal of center frequency).				
*3	The input clock cycle jitter is difference in period between adjacent cycles.				
*4	The jitter characteristics must meet both t_{Cjper} and $t_{CJcycle}$ characteristics.				
*	Ensure that clock overshoot/undershoot does not exceed absolute maximum ratings in Table 6.1.				

6.4.3 Power-on / Reset Timing

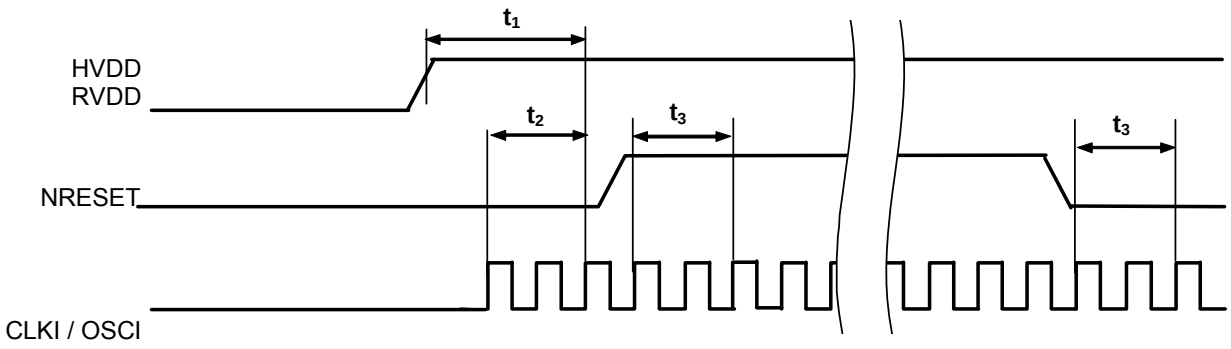


Figure 6.3 Power on / reset timing

Table 6.9 Power on / reset timing

Symbol	Item		Min.	Typ	Max.	Unit
t_1	Minimum delay from the HVDD power-on to the CLKI/OSCI rising edge before NRESET release.	Input clock source: CLKI	100	-	-	μs
		Input clock source: OSCI *2	-	1	-	s
t_2	The minimum NRESET assertion on system power up.		2	-	-	T_{OSC} (*1)
t_3	NRESET synchronization time (Number of clock cycles before the reset signal is applied internally.)		2	-	-	T_{OSC} (*1)
*1	T_{OSC} is the CLKI / OSCI clock period.					
*2	Oscillation characteristics change depending on conditions such as components used (oscillator, Rf, Rd, Cg, Cd), board pattern, and rising time of supplied voltage. Use this characteristics as reference values.					

Note: The circuit must be initialized with NRESET after initiating power supply. The internal circuit state cannot be guaranteed when switching the HVDD from off to on, due to power supply noise and other factors.

6.4.4 Command Receipt Timing

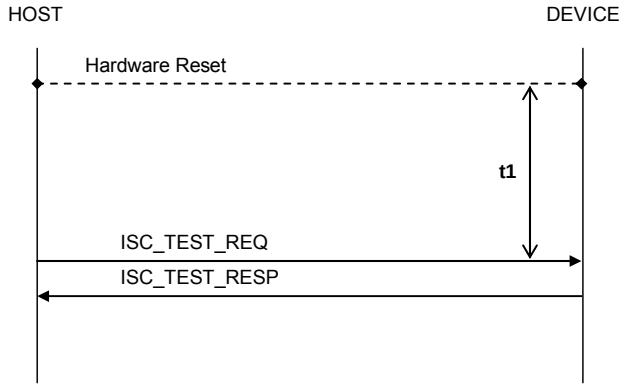


Figure 6.4 Command receipt timing

The system starts up after t_1 time following hardware reset.

Then ISC_TEST_REQ/RESP message flow can be used.

Table 6.10 Command receipt timing

Symbol	Parameter	Min.	Max.	Unit
t_1	Length of time from initialization to message acceptance ready state (*1)	120	-	ms
*1	There should be no problem about sending padding bytes during the t_1 period.			

6.4.5 Serial Interface (Clock Synchronous)

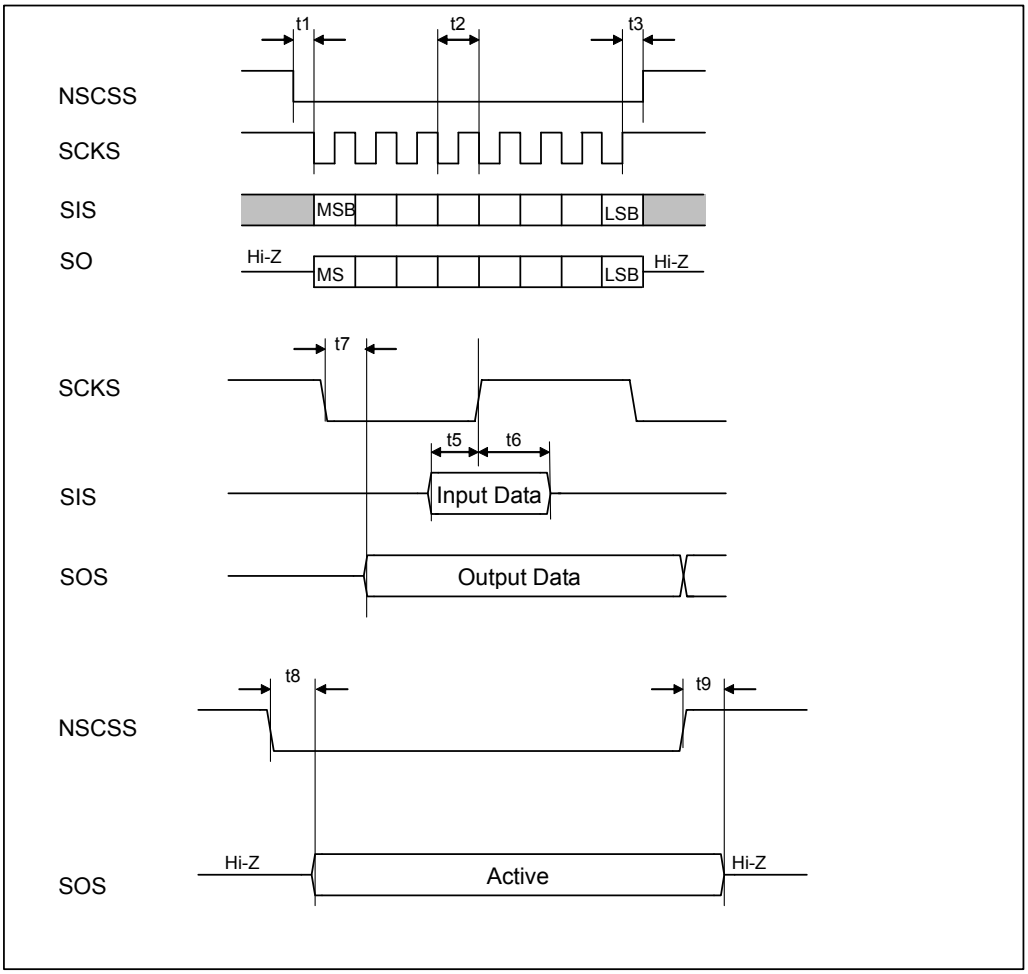


Figure 6.5 Clock synchronous serial interface timing

Table 6.11 Clock synchronous serial interface timing

Symbol	Parameter	Min.	Max.	Unit
t_1	NSCSS falling time to SCKS falling time	100	-	ns
t_2	SCKS cycle time	1.0	-	µs
t_3	SCKS rising time to NSCSS rising time	100	-	ns
t_5	SIS setup time	30	-	ns
t_6	SIS hold time	30	-	ns
t_7	SCKS falling time to SOS going active	-	60	ns
t_8	NSCSS falling time to SOS going active	-	60	ns
t_9	NSCSS rising time to SOS going Hi-Z	-	60	ns

6.4.6 Serial Interface (I2C)

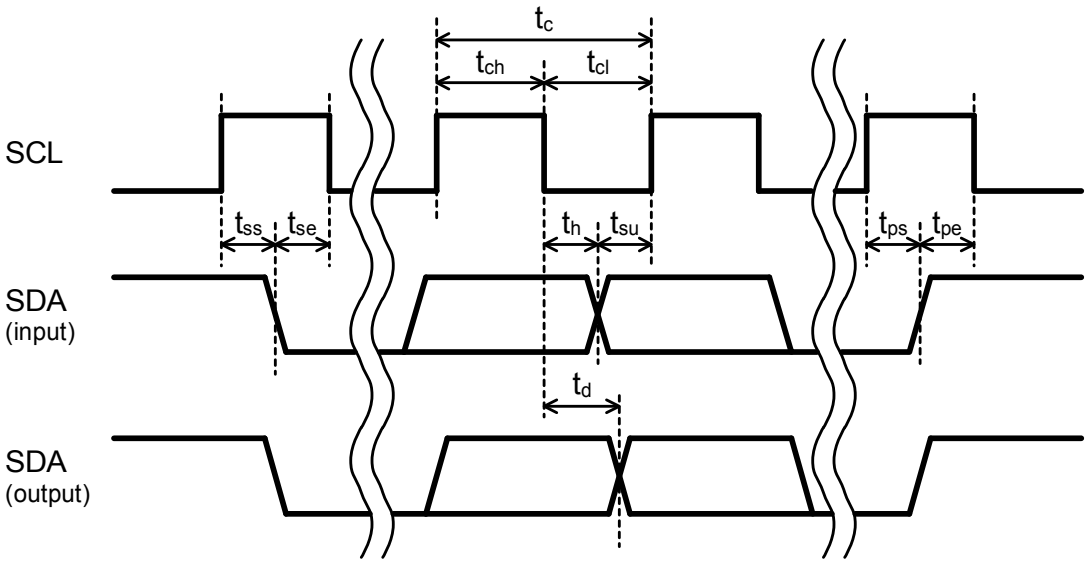


Figure 6.6 I2C timing

Table 6.12 Serial interface (I2C) timing

Symbol	Parameter	Min.	Max.	Unit
t_c	SCL clock frequency (*1)	12.0	-	µs
t_{ch}	SCL clock pulse width high	6.0	-	µs
t_{cl}	SCL clock pulse width low (*1)	6.0	-	µs
t_{su}	SDA input setup time	0.5	-	µs
t_h	SDA input hold time	0	-	µs
t_d	SDA output delay time (*1)	-	5.5	µs
t_{ss}	START condition start time	2.5	-	µs
t_{se}	START condition completion time	2.5	-	µs
t_{ps}	STOP condition start time	2.5	-	µs
t_{pe}	STOP condition completion time	2.5	-	µs
*1	These numerical values are based on the I2C bus rising time of 480 ns or less. It should be noted that the numerical values will be greater if the I2C bus rising time exceeds 480 ns due to the load capacity and pull-up resistance.			

7. External Connection Examples

7.1 System Clock

The S1V3S344 system clock frequency can be set to either 32.768 kHz or 12.288 MHz. Likewise, the clock source can be set to either direct input (input from CLKI pin) or oscillator (connected to OSCI/OSCO pin). The oscillator, however, can be used with 32.768 kHz only. External connection examples are shown below for various clock supply configurations.

7.1.1 Direct Input

Figure 7.1 shows an example of an external connection in which the clock signal input to the CLKI pin is used as the clock source.

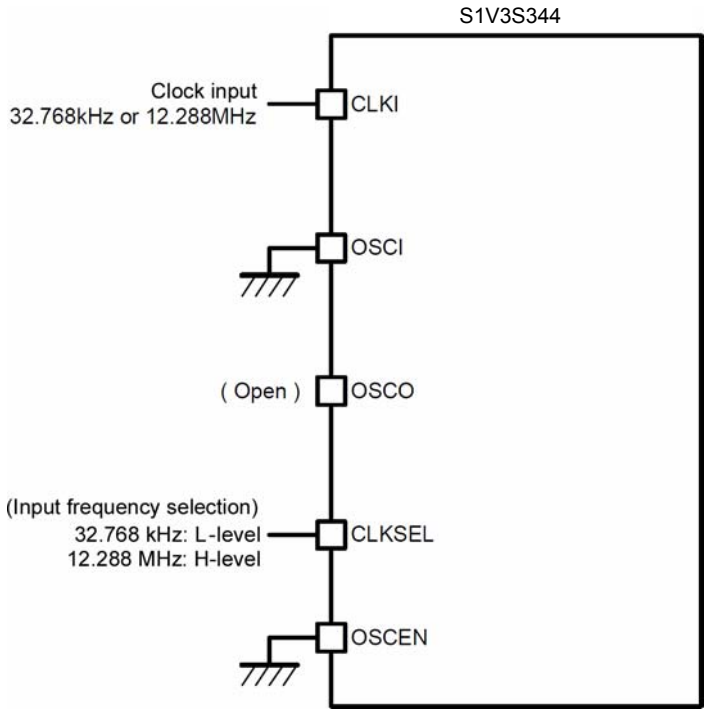


Figure 7.1 System clock external connection example (CLKI pin)

The CLKI pin receives 32.768 kHz or 12.288 MHz clock signal input generated by an oscillator.

The CLKSEL pin should be set to Low level for 32.768 kHz and to High level for 12.288 MHz.

The OSCEN pin should be set to Low level.

The OSCI pin should be set to Low level.

The OSCO pin should not be connected.

Note that the asynchronous serial interface (UART) is not available if the system clock frequency is set to 12.288 MHz.

7.1.2 Oscillator (32.768 kHz)

Figure 7.2 shows an example of an external connection in which a 32.768 kHz oscillator is used as the clock source.

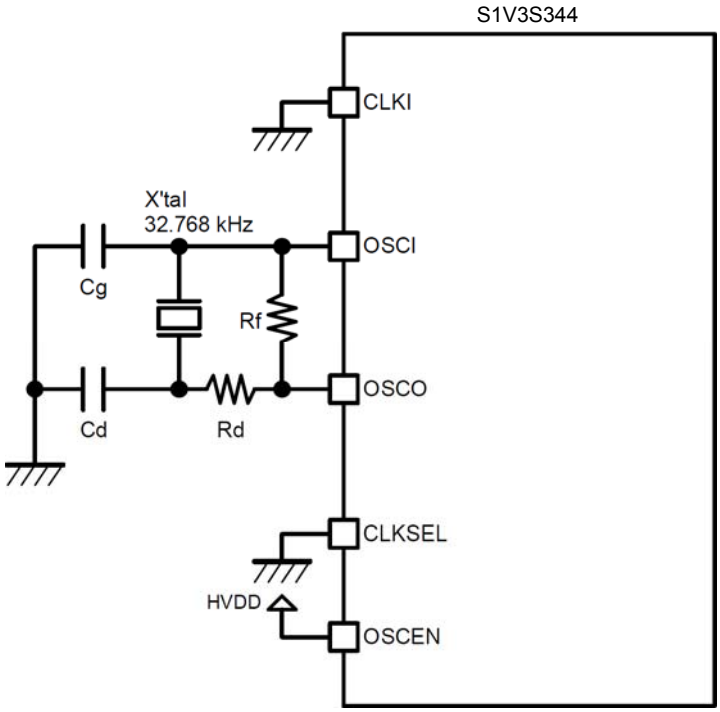


Figure 7.2 Example of external system clock connection (32.768 kHz oscillator)

The 32.768 kHz oscillator and oscillator circuit is connected to the OSCI and OSCO pins as shown in Figure 7.2.

The CLKSEL pin should be set to Low level.

The OSCEN pin should be set to High level.

The CLKI pin should be set to Low level.

Table 7.1 gives typical external circuit constants for a 32.768 kHz oscillator. These will vary, depending on individual oscillator characteristics (e.g., components and circuit board patterns used). The values given in Table 7.1 are examples only and do not constitute performance guarantees.

Table 7.1 Typical 32.768 kHz oscillator external circuit constants

X'tal	32.768 kHz oscillator	Crystal (Epson Toyocom FC-135)
Cg	Gate capacity	10 pF
Cd	Drain capacity	10 pF
Rf	Feedback resistance	10 MΩ
Rd	Drain resistance	200 kΩ

7.2 Serial Interface

7.2.1 Clock Synchronous

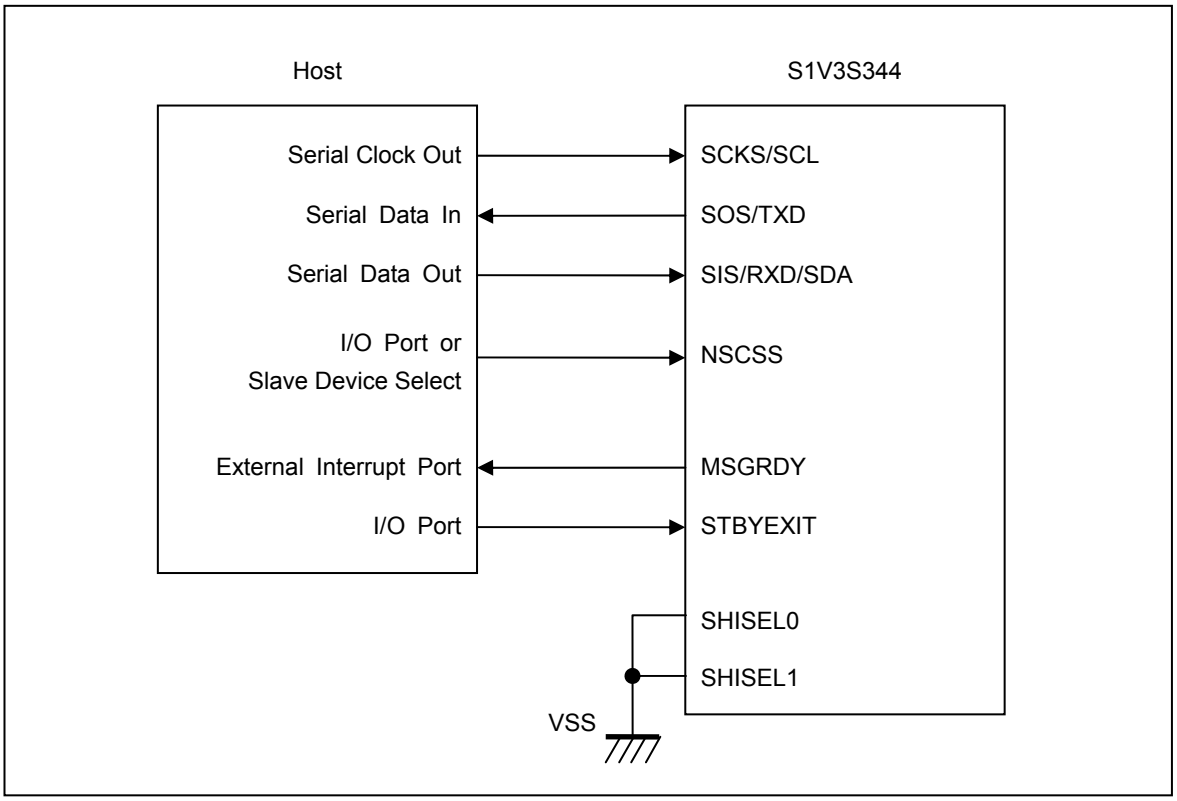


Figure 7.3 Example of serial interface external connection (clock synchronous)

When using a clock synchronous serial interface, set both input pins SHISEL0 and SHISEL1 to Low level.

SOS is active when NSCSS is Low level. SOS will be high impedance when NSCSS is High level. Multiple slave devices can be connected through a general output port or host serial interface slave device selection signal as shown in Figure 7.3. When controlling the NSCSS pin via a host general port, set to Low level immediately before sending a message and to High level once a message is received.

MSGRDY is an output signal that indicates a command from the S1V3S344 is ready to be sent. This signal can be used as an interrupt signal sent to the host to warn the host to reduce loads to prepare for message receipt. For more information on MSGRDY output timing, refer to *S1V3034x Series Message Protocol Specification*.

STBYEXIT is an input signal to implement recovery from standby mode to normal operating mode. For more information on STBYEXIT input timing, refer to *S1V3034x Series Message Protocol Specification*.

7.2.2 Asynchronous (UART)

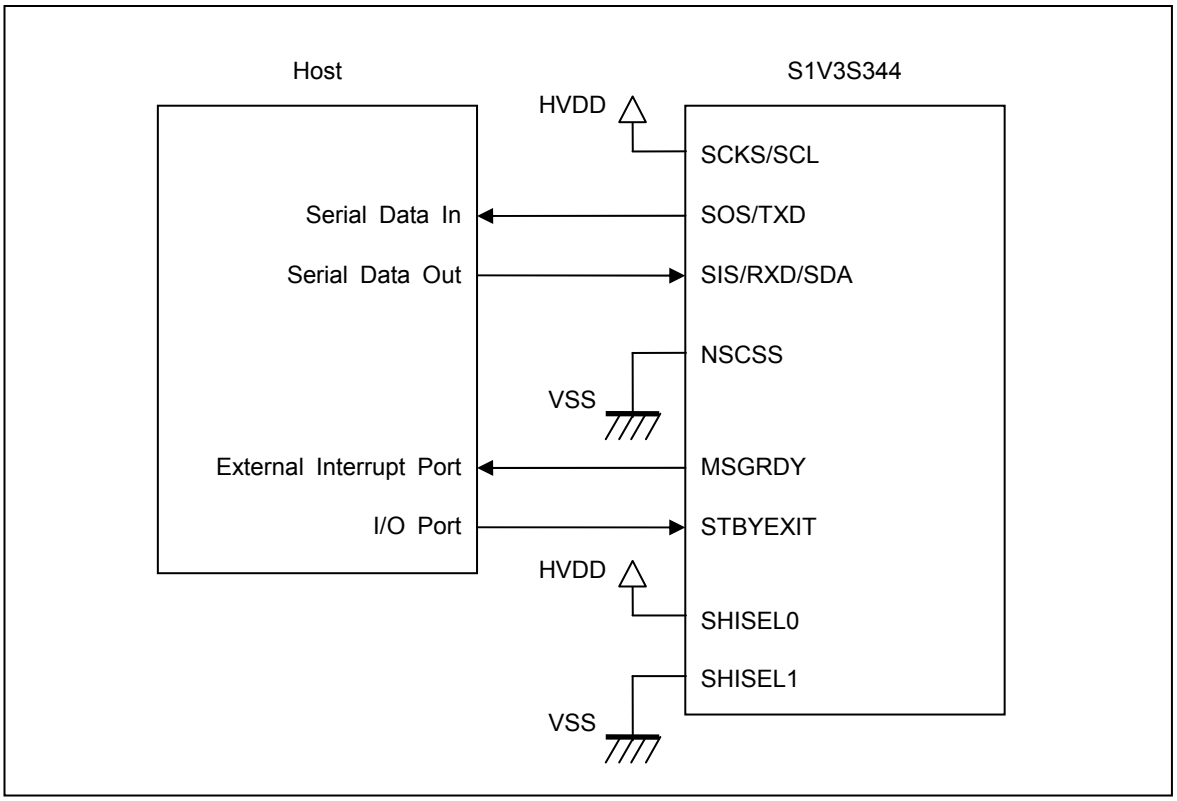


Figure 7.4 Serial interface external connection example (asynchronous)

When using an asynchronous serial interface (UART), the SHISEL0 input pin should be set to High level and SHISEL1 should be set to Low level. Note that the UART interface is not available when the system clock frequency is 12.288 MHz.

The initial interface settings are as shown below.

Start bit length: 1 bit

Stop bit length: 1 bit

Parity bit: None

Baud rate: 9.6 kbps

The interface settings can be changed using the ISC_UART_CONFIG_REQ message. Interface settings set via this message will be maintained until a hardware reset. A hardware reset restores interface settings to the initial default values shown above. The ISC_UART_CONFIG_REQ message can be used if necessary. For additional information, refer to *S1V3034x Series Message Protocol Specification*.

MSGRDY is an output signal indicating that a command to be sent from the S1V3S344 is ready to be sent. For more information on the data receiving flow on the host side and the MSGRDY output timing, refer to *S1V3034x Series Message Protocol Specification*.

STBYEXIT is an input signal used to implement recovery from standby mode to normal operating mode. For more information on the STBYEXIT input timing, refer to *S1V3034x Series Message Protocol Specification*.

7.2.3 I2C

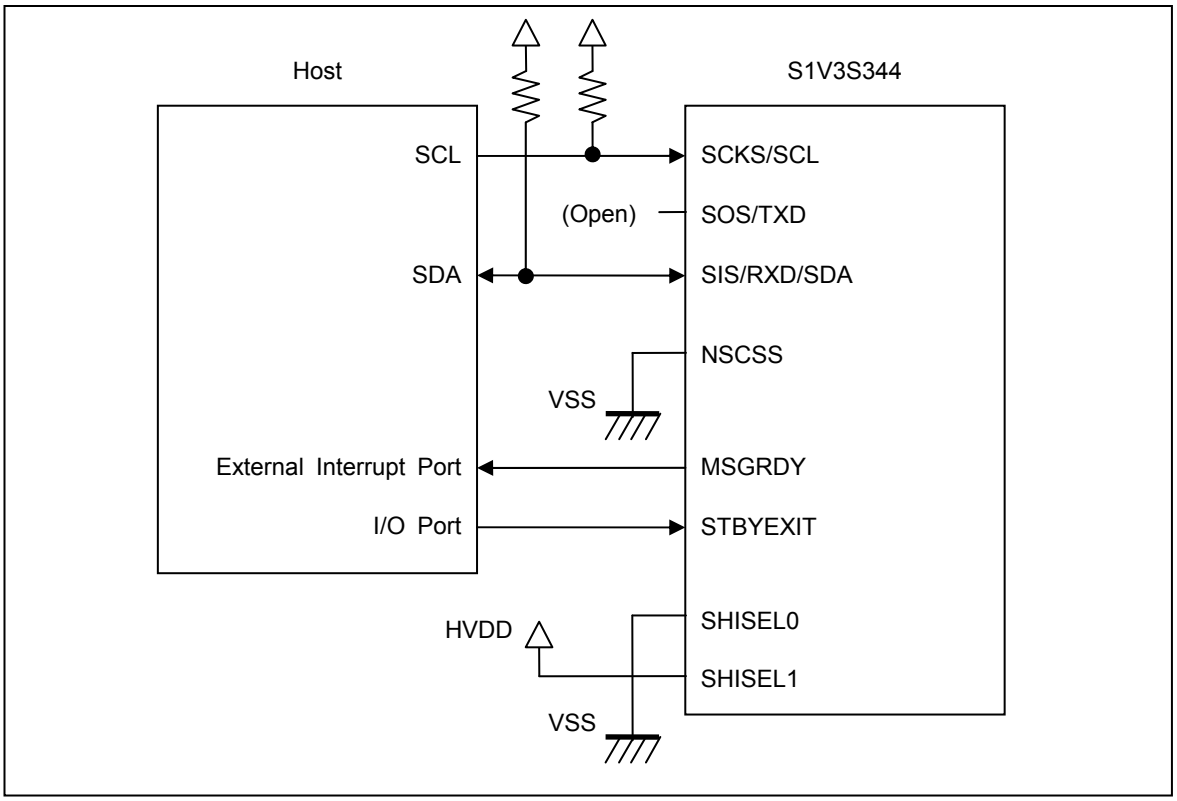


Figure 7.5 Serial interface external connection example (I2C)

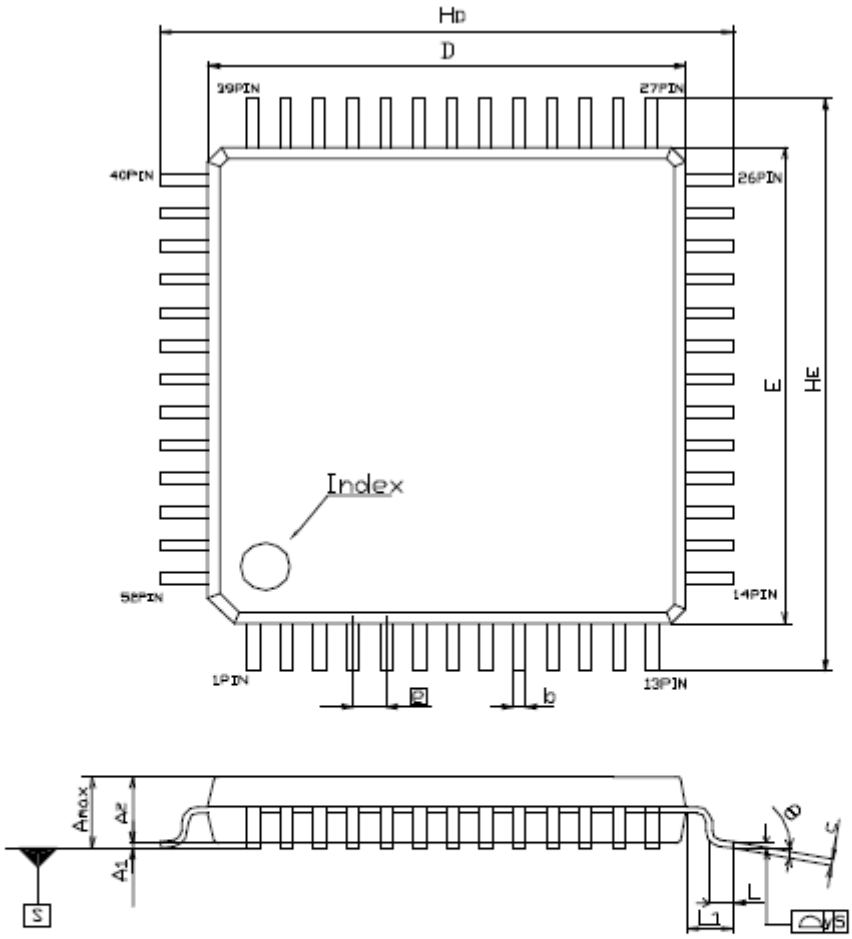
If I2C is used, set the SHISEL0 input pin to Low level and SHISEL1 to High level.

MSGRDY is an output signal indicating that a command to be sent from the S1V3S344 is ready to be sent. For more information on the data receiving flow on the host side and the MSGRDY output timing, refer to *S1V3034x Series Message Protocol Specification*.

STBYEXIT is an input signal used to implement recovery from standby mode to normal operating mode. For more information on the STBYEXIT input timing, refer to *S1V3034x Series Message Protocol Specification*.

8. Package Dimensions

8.1 QFP13-52



Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	–	10	–
D	–	10	–
Amax			1.7
A1		0.1	
A2	–	1.4	–
e		0.65	
b	0.2	–	0.4
c	0.09	–	0.2
θ	0°		10°
L	0.3	–	0.75
L1		1	
HE	–	12	–
HD	–	12	–
y	–	–	0.1

1 – 1nn

9. Reference Material

9.1 Circuit Application Example

Figure 9.1 shows a typical S1V3S344 circuit application.

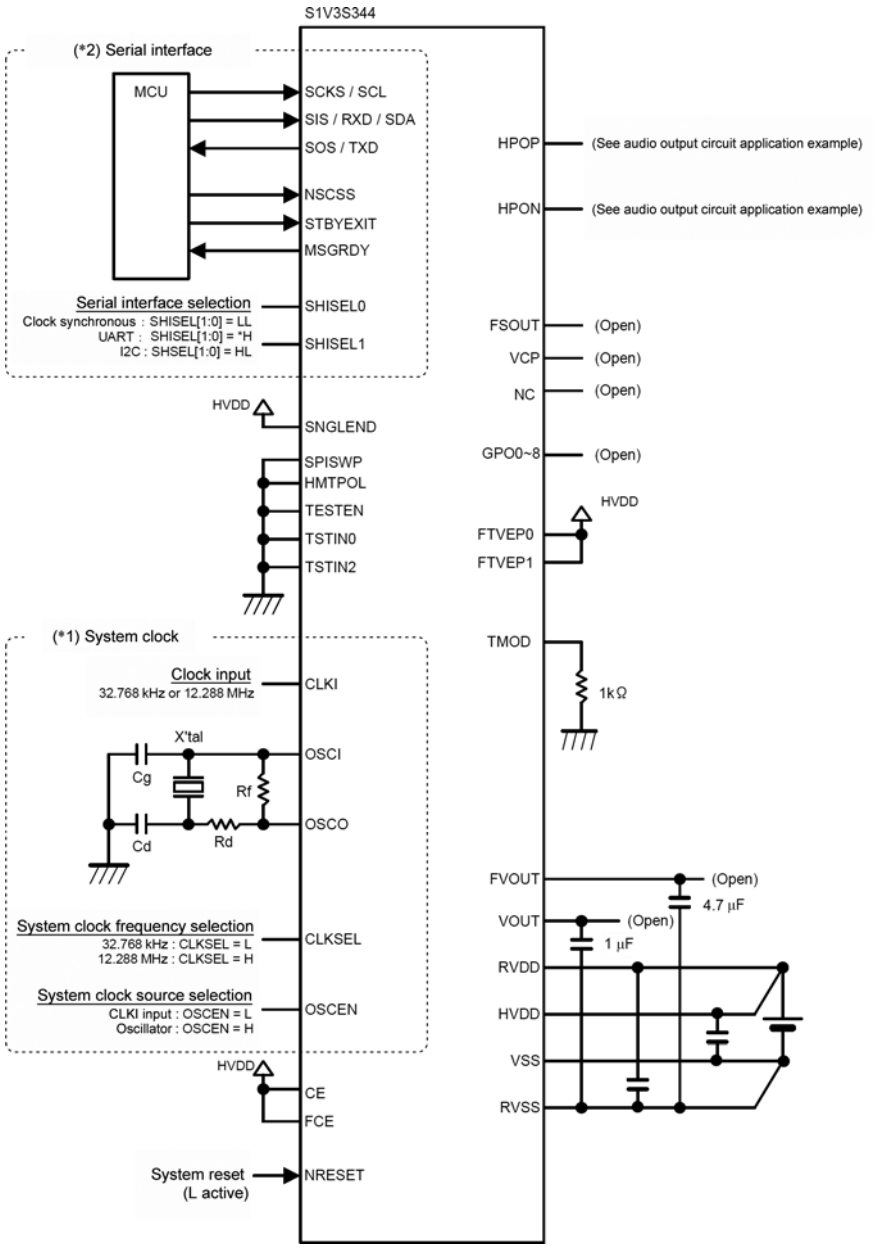


Figure 9.1 S1V3S344 circuit application example

*1: The system clock input unit connection configuration will vary, depending on the clock frequency and clock source used. Refer to section 7.1 for more information.

*2: The serial interface connection configuration will vary, depending on the interface type used. Refer to section 7.2 for additional information.

*3: The bypass capacitor will vary depending on the system, but should be several μF to several tens of μF.

9.2 Circuit Application Example (Audio Output Unit)

Figure 9.2 shows a typical audio output unit circuit application.

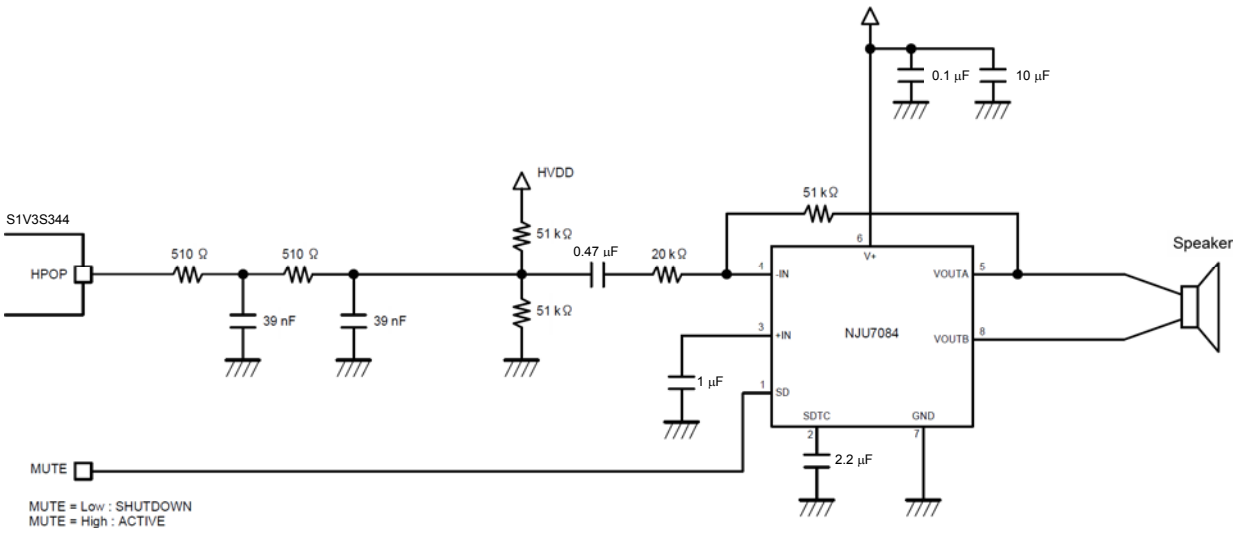


Figure 9.2 S1V3S344 circuit application example (audio output unit)

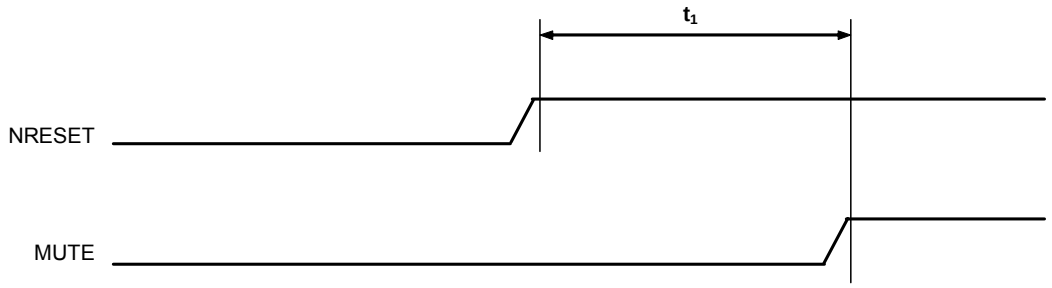
The connection from the HPOP/HPON pins to the secondary LPF (510 Ω, 39 nF) should be as short as possible. The secondary LPF capacitor (39 nF) GND connection to the VSS should also be as short as possible.

The speaker amplifier peripheral circuit and circuit constants shown in Figure 9.2 are provided solely for reference and do not constitute performance guarantees.

9.3 Mute Start/Release Timing

It is recommended to control the mute function of the speaker amplifier by using the general-purpose input/output port in order to minimize noise at power ON/OFF and in standby. The following shows an example of mute control timing in each operation condition.

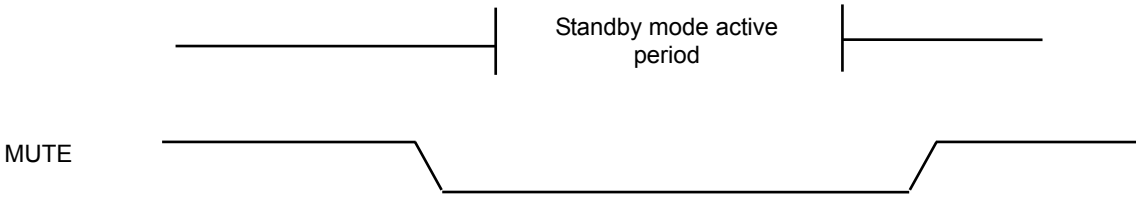
9.3.1 System Reset Active ⇒ Release



Symbol	Item	Min.	Max.	Unit
t_1	NRESET release time to MUTE release time	150	-	ms

Note: In the above timing chart, the MUTE pin is at the Low level and MUTE is active.

9.3.2 Standby Mode



The following shows an example of the MUTE control flow before and after standby mode.

- Transition to standby mode
  MUTE enabled → STANDBY_ENTRY_REQ issued → STBYEXIT: High
- End of standby mode
  STBYEXIT: Low → STANDBY_EXIT_IND received → MUTE released

Note: In the above timing chart, the MUTE pin is at the Low level and MUTE is active.

* Refer to the *Message Protocol Specification* for details of standby mode.

9.4 Power Supply Precautions

Always initialize the circuit with NRESET after initiating power supply. The internal circuit state cannot be guaranteed when switching the HVDD from off to on due to power supply noise and other factors.

CMOS devices may suffer from what is known as “latch-up.” This is a phenomenon in which the PNPN bonds (thyristor configuration) inside the CMOS IC conduct, resulting in large currents between VDD and VSS and ultimately damaging the CMOS.

Latch-up occurs when the voltage applied to the input/output pins exceeds rated values, resulting in large currents within the component, or when the VDD pin voltage exceeds the ratings, causing internal components to yield. If the voltage exceeds the ratings even momentarily in these cases, a large current will arise between VDD and VSS once latch-up occurs, resulting in potential overheating and smoke generation. Always observe the following precautions:

(1) Never raise the input/output pin voltage level above the supply voltage or above the range specified for electrical characteristics. Avoid lowering below VSS.

(2) Make sure the device is not subject to abnormal noise.

(3) The potential for unused input pins should be pegged to VDD or VSS.

(4) Do not short-circuit the output.

9.5 Clock Direct Input Precautions

Noise will be input to the power supply if the overshoot or undershoot in the clock is excessive when using an external direct clock input. This may cause the internal regulator output to fluctuate, possibly resulting in internal circuit damage or malfunction.

Clock overshoot and undershoot must be kept within the input voltage range indicated in Section "6.1 Absolute Maximum Ratings." If overshoot or undershoot is present, this should be addressed using a damping resistance or low pass filter.

The same prevention measures are required for external signals other than the clock external input, but particular caution is necessary for the clock due to the high frequency.

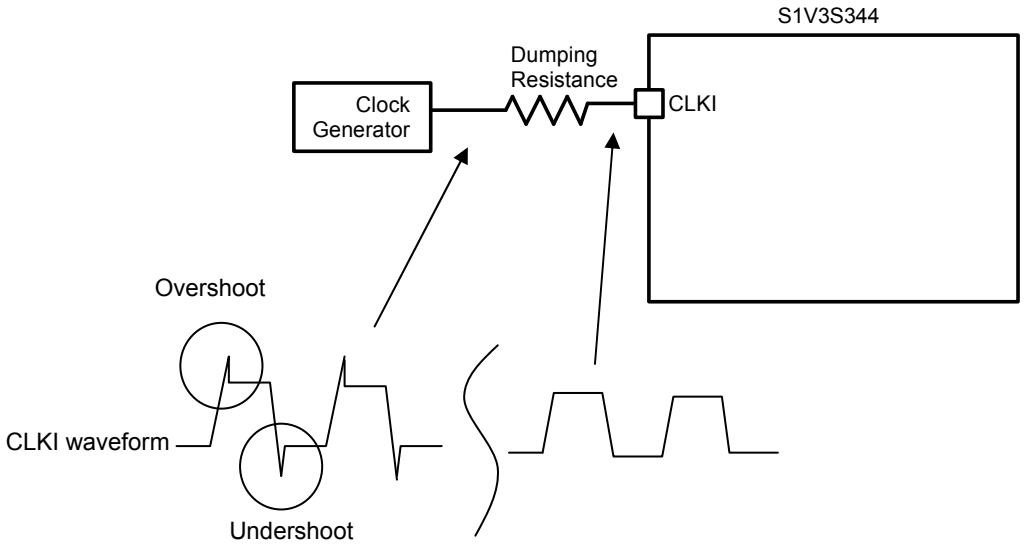


Figure 9.3 Typical clock input overshoot/undershoot prevention measures

9.6 Precautions on Mounting

The following shows the precautions when designing the board and mounting the IC.

9.6.1 Oscillation Circuit

Oscillation characteristics change depending on conditions such as components used (oscillator, Rf, Rd, Cg, Cd) and board pattern. In particular, when a ceramic or crystal oscillator is used, evaluate the components adequately under real operating conditions by mounting them on the board before the external resistor (Rf, Rd) and capacitor (Cg, Cd) values are finally decided.

Disurbances of the oscillation clock due to noise may cause a malfunction. To prevent this, the following points should be taken into consideration.

- Components that are connected to the OSCI and OSCO pins, such as oscillator, resistors and capacitors, should be connected in the shortest line.
- Whenever possible, configure digital signal lines with at least three millimeters clearance from the OSCI and OSCO and the components and lines connected to these pins. In particular, signals thet are switched frequently must not be placed near these pins, components, and lines. The same applies to all layers on the multi-layered board as the distance between the layers is around 0.1 to 0.2 mm. Furthermore, do not configure digital signal lines in parallel with these components and lines when arranging them on the same or another layer of the board. Such an arrangement is strictly prohibited, even with clearance of three millimeters or more. Also, avoid arranging digital signal lines across these components and signal lines.
- Shield the OSCI and OSCO pins and lines connected to those pins as well as the adjacent layers of the board using VSS. As shown in Figure 9.4, shield the wired layers as much as possible. Whenever possible, make the whole adjacent layers the ground layers, or ensure there is adequate shielding to a radius of five millimeters around the above pins and lines. Do not configure digital signal lines in parallel with components and lines even if such components and lines on other layers.

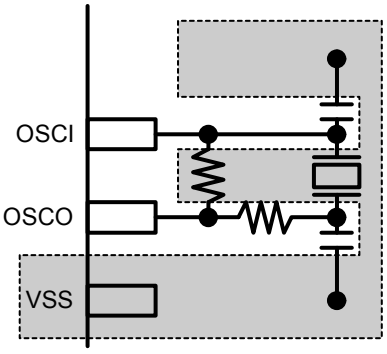


Figure 9.4 Example of oscillation circuit VSS pattern

9.6.2 Reset Circuit

The power-on reset signal which is input to the NRESET pin changes depending on conditions (power rise time, component used, board pattern, etc.). Decide the constant of the capacitor and resistor after enough tests have been completed with the apprication product. With regard to the pull-up resistance of the NRESET pin, if the impedance is high, noise can generate a malfunction; therefore, the constants must be determined in careful consideration of resistance value variations.

9.6.3 Power Supply Circuit

Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

- The power supply should be connected to the HVDD/RVDD and VSS/RVSS pins with patterns as short and large as possible.
- When connecting between the HVDD/RVDD – VSS/RVSS pins with a bypass capacitor, the HVDD/RVDD and VSS/RVSS pins should be connected as short as possible. The bypass capacitor will vary depending on the system, but should be several μF to several tens of μF.
- Connect a 1 μF bypass capacitor between VOUT and RVSS, and connect the VOUT and RVSS pins as short as possible.
- Connect a bypass capacitor of at least 4.7 μF between FVOUT and RVSS and ensure that the connection between the FVOUT and RVSS pins is as short as possible.

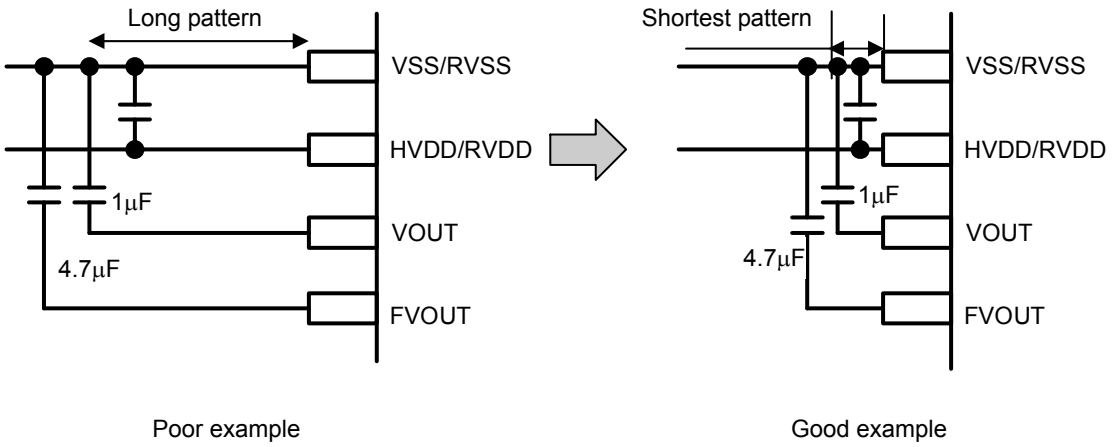


Figure 9.5 Bypass capacitor connection example

9.6.4 Arrangement of Signal Lines

In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.

When a signal line is pallalel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.

9.6.5 Noise-Induced Erratic Operations

If erratic IC operations appear to be attributable to noise, consider the following three points.

- NRESET pin
  Low-level noise on this pin resets the IC. However, the IC may not always be reset normally, depending on the input waveform. Due to circuit design, this situation tends to occur when the reset input is in the high state, with high impedance.
- SCKS pin
  The SCKS pin is a synchronous clock input of a clock synchronous serial interface. If a noise goes into this pin, depending on the input waveform, it will be recognized as valid data, and will become the cause of malfunction. When connecting between the host and serial interface (SCKS, SIS, SOS and NSCSS) pins, these should be connected as short as possible.
- Power supplies
  If noise lower than the rated voltage enters one of these power-supply lines, the IC may operate erratically. Take collective measures in board design; for example, by using soild patterns for power supply lines, adding decoupling capacitors to eliminate noise, or incorporating surge/noise counteracting devices into the power supply lines.

9.6.6 Others

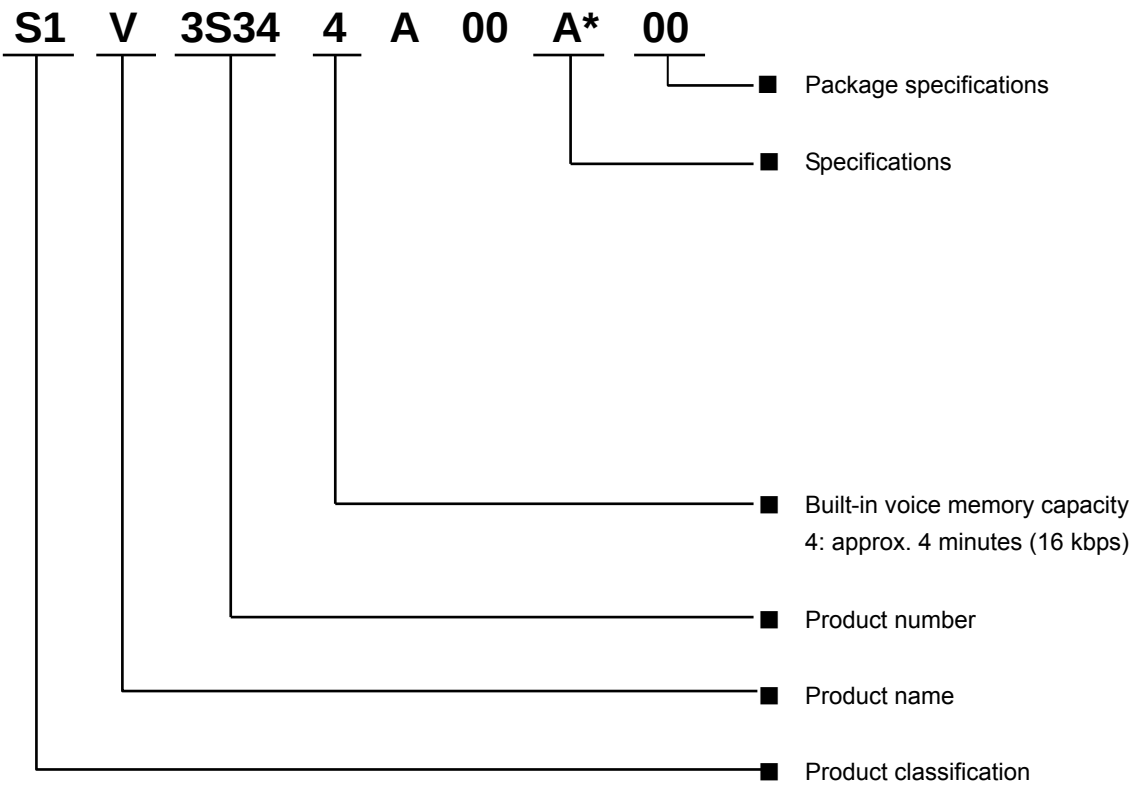
The IC is designed with a fundamental reliability satisfying EIAJ and MIL standards, but the following precautions must be observed for product mounting.

Since OSCI and OSCO pins are constructed to use the internal transistors directly, the pins are susceptible to mechanical damage during the board-mounting process. Moreover, the pins may also be susceptible to electraical damage caused by such disturbances (listed below) whose electrical strength are varying gradually with time and can exceed the absolute maximum rated voltage (2.5 V) of the IC.

- Electromagnetic induction noise from the utility power supply in the reflow process during board-mounting, rework process after board-mounting, or individual characteristics evaluation (experimental confirmation), and
- Electromagnetic induction noise fro the tip of a soldering iron

Especially when using a soldering iron, make sure that the IC GND and soldering iron GND are at the same potential before soldering.

9.7 Product Code Numbering



Revision History

Date	Revision details			
	Rev.	Page	Type	Details
03/05/2009	1.00	All	New	First issue
25/01/2010	1.1	20	Modify	section 6.4.3 : t1 (Input clock source: OSCI) Typ=1s
		20	Add	section 6.4.3 : Add comment *2
		30	Add	section 9.1 : Add comment *3

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Document Code: 411707901
First Issue April 2009ⓓ
Revised January 2010 in JAPAN