DATA SHEET

PCA9556

Octal SMBus and I^2C registered interface

Product data
Supersedes data of 2000 Nov 13

2002 Mar 28

Philips
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Octal SMBus and I²C registered interface PCA9556

FEATURES

- SMBus compliance with fixed 3.3V voltage levels
- Operating power supply voltage range of 3.0 V – 5.5 V
- Active high polarity inverter register
- Each I/O is configurable as an input or output
- Active low reset pin
- Low leakage current on power-down
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- High impedance open drain on I/O0
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

The PCA9556 is a silicon CMOS circuit which provides parallel input/output expansion for SMBus applications. The PCA9556 consists of an 8-bit input port register, 8-bit output port register, and an SMBus interface. It has low current consumption and a high impedance open drain output pin, I/O0.

The SMBus system master can reset the PCA9556 in the event of a timeout by asserting a LOW on the reset input. The SMBus system master can also invert the PCA9556 inputs by writing to the active HIGH polarity inversion bits. Finally, the system master can enable the PCA9556's I/Os as either inputs or outputs by writing to the configuration register.

The power-on reset puts the registers in their default state and initializes the SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part.

The PCA9557 8-bit I²C SMBus I/O port with reset is the higher performance pin-for-pin replacement for the PCA9556.

PIN CONFIGURATION

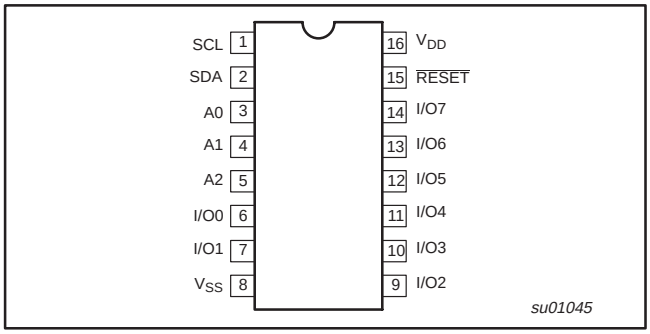


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	SCL	Serial clock line
2	SDA	Serial data line
3	A0	Address input 0
4	A1	Address input 1
5	A2	Address input 2
6	I/O0	I/O0 (open drain)
7	I/O1	I/O1
8	V_{SS}	Supply GROUND
9–14	I/O2–I/O7	I/O2 to I/O7
15	$\overline{\text{RESET}}$	External reset (active LOW)
16	V_{DD}	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
16-Pin Plastic TSSOP	–40 to +85 °C	PCA9556PW	SOT403-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.
SMBus as specified by the Smart Battery System Implementers Forum is a derivative of the Philips I²C patent.
I²C is a trademark of Philips Semiconductors Corporation.

BLOCK DIAGRAM

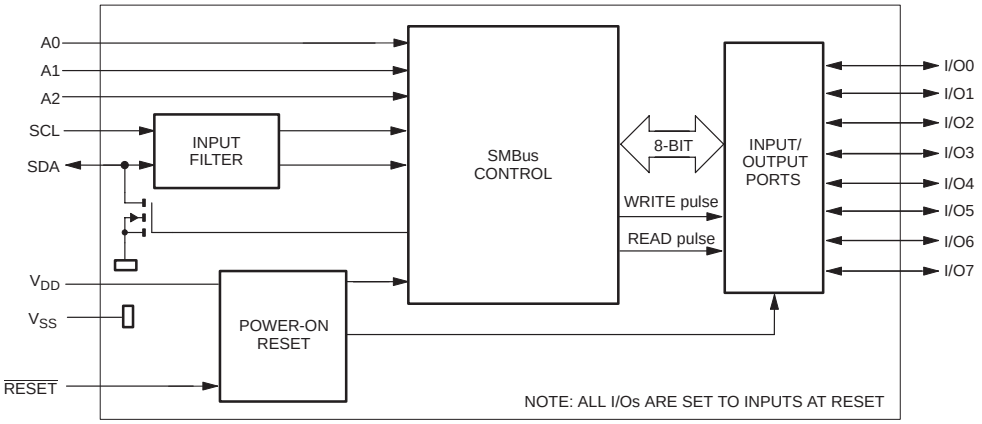


Figure 2. Block diagram

SYSTEM DIAGRAM

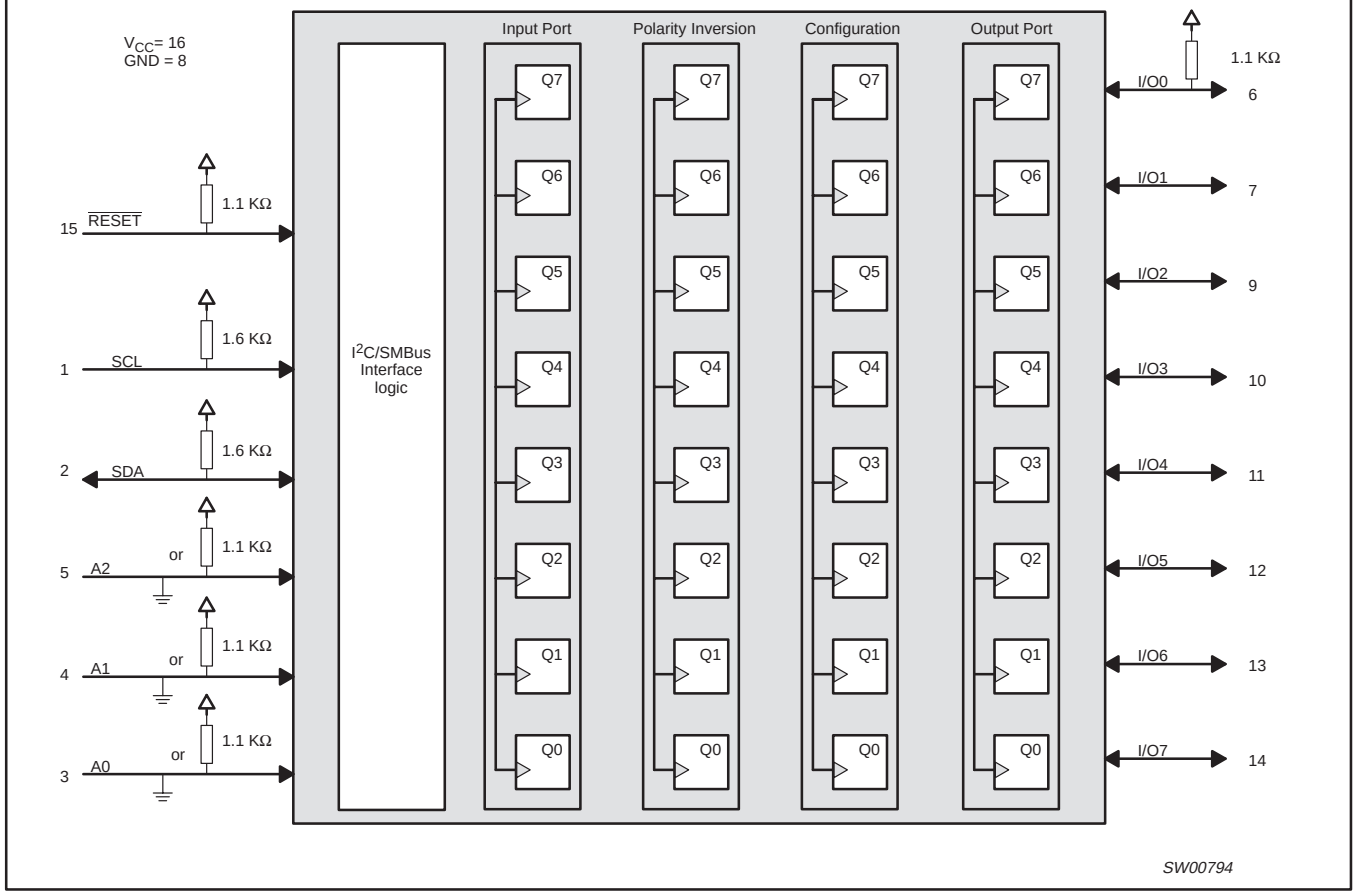


Figure 3. System diagram

REGISTERS

Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0 — Input Port Register

I7	I6	I5	I4	I3	I2	I1	I0

This register is an read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by register 3. Writes to this register have no effect.

Register 1 — Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	0	0	0	0	0	0	0	0

This register reflects the outgoing logic levels of the pins defined as outputs by register 3. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Register 2 — Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	1	1	1	1	0	0	0	0

This register enables polarity inversion of pins defined as inputs by register 3. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Register 3 — Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output.

RESET

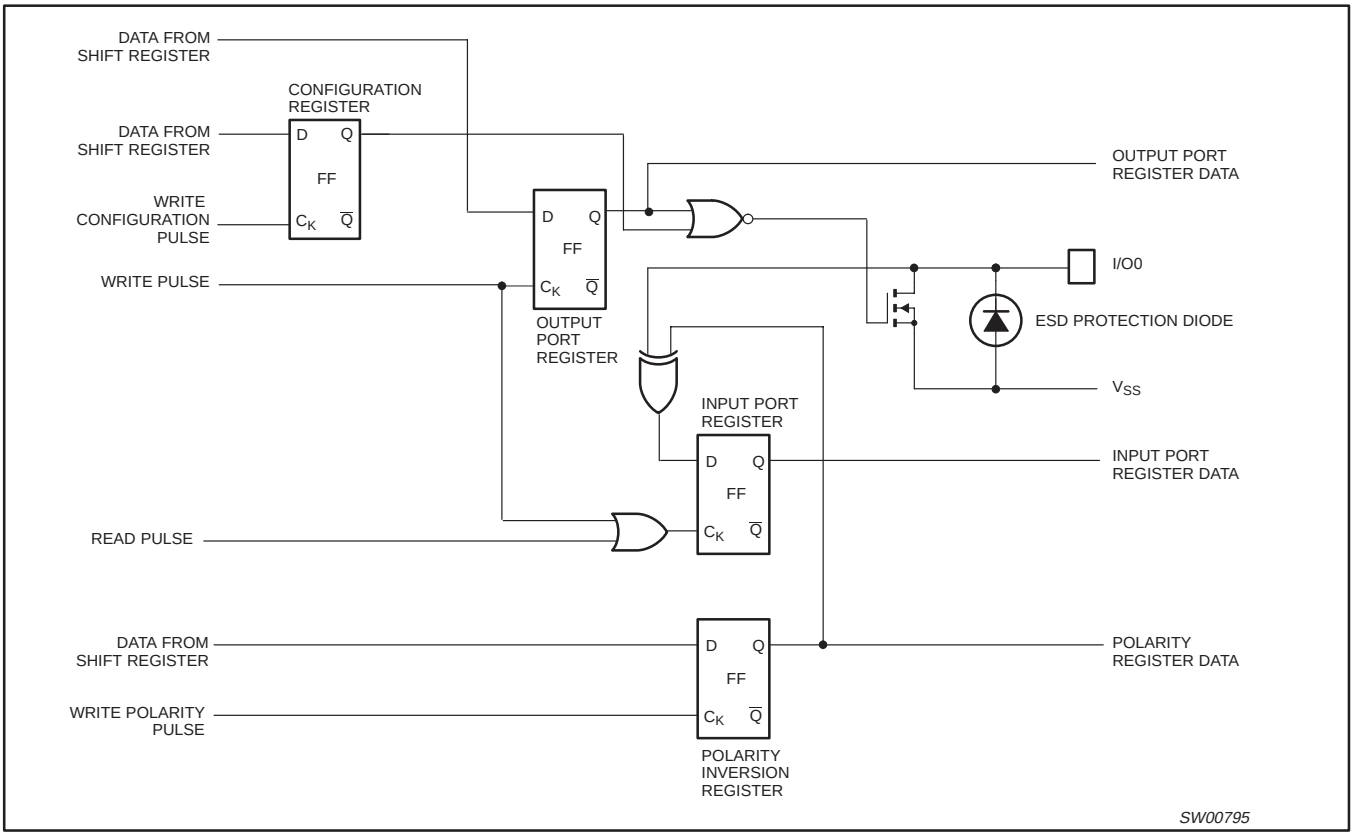
Power-on Reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9556 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9556 registers and SMBus state machine will initialize to their default states.

External Reset

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of T_W. The PCA9556 registers and SMBus/I²C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again high. This input typically requires a pull-up to 3.3 V V_{CC}.

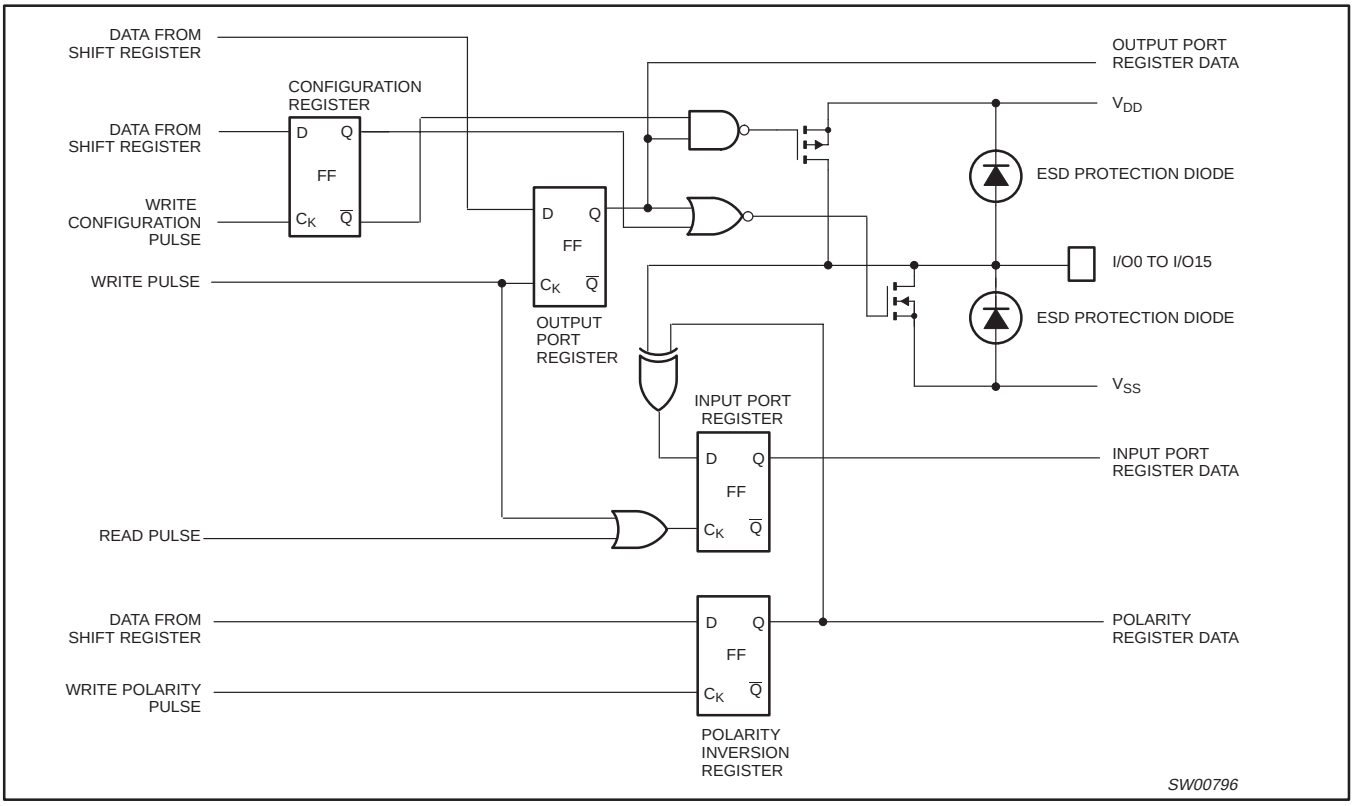
SIMPLIFIED SCHEMATIC OF I/O0



NOTE: On power–up or reset, all registers return to default values.

Figure 4. Simplified schematic of I/O0

SIMPLIFIED SCHEMATIC OF I/O1 TO I/O7



NOTE: On power–up or reset, all registers return to default values.

Figure 5. Simplified schematic of I/O1 to I/O7

SMBus Address

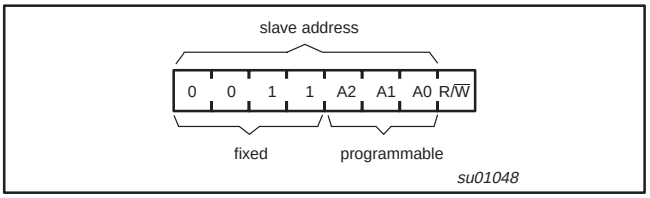


Figure 6. PCA9556 address

SMBus Transactions

Data is transmitted to the PCA9556 registers using Write Byte transfers (see Figures 7 and 8). Data is read from the PCA9556 registers using Read and Receive Byte transfers (see FIgures 9 and 10).

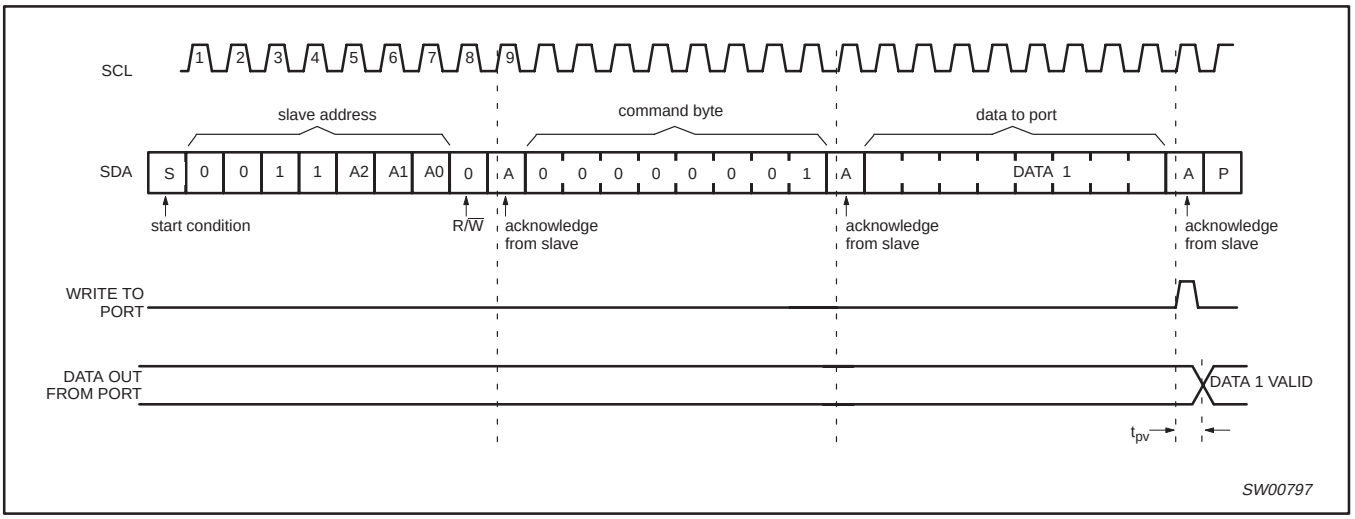


Figure 7. WRITE to output port register via Write Byte Protocol

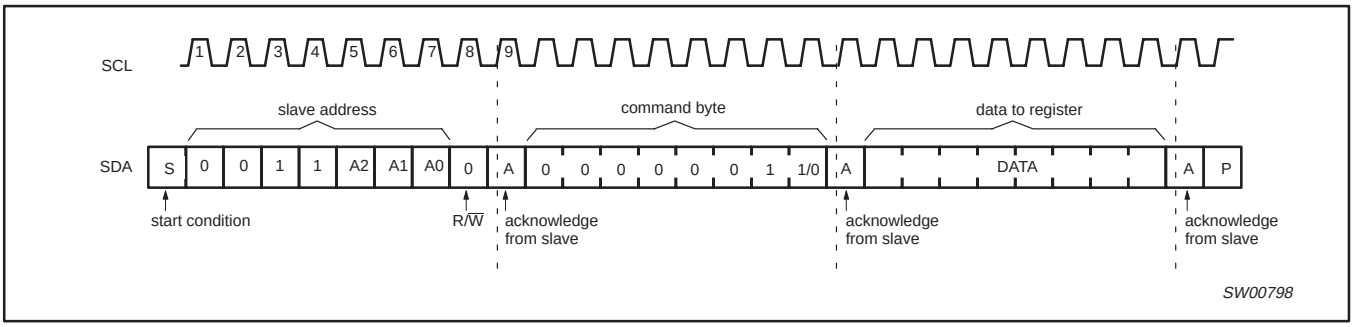


Figure 8. WRITE to I/O configuration or polarity inversion registers via Write Byte Protocol

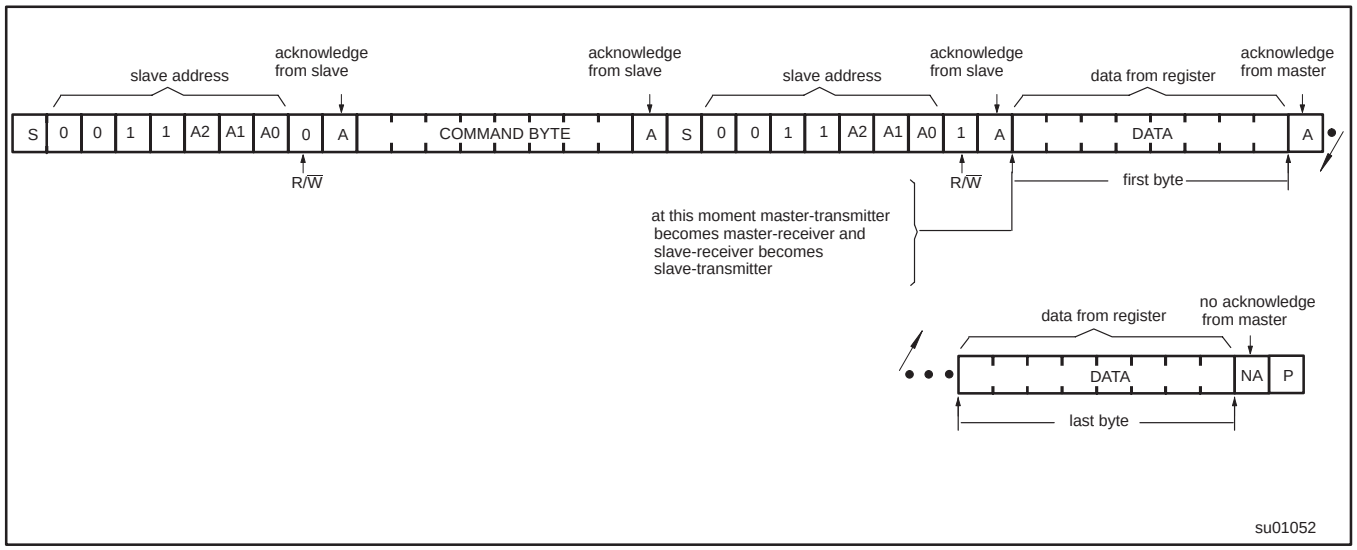
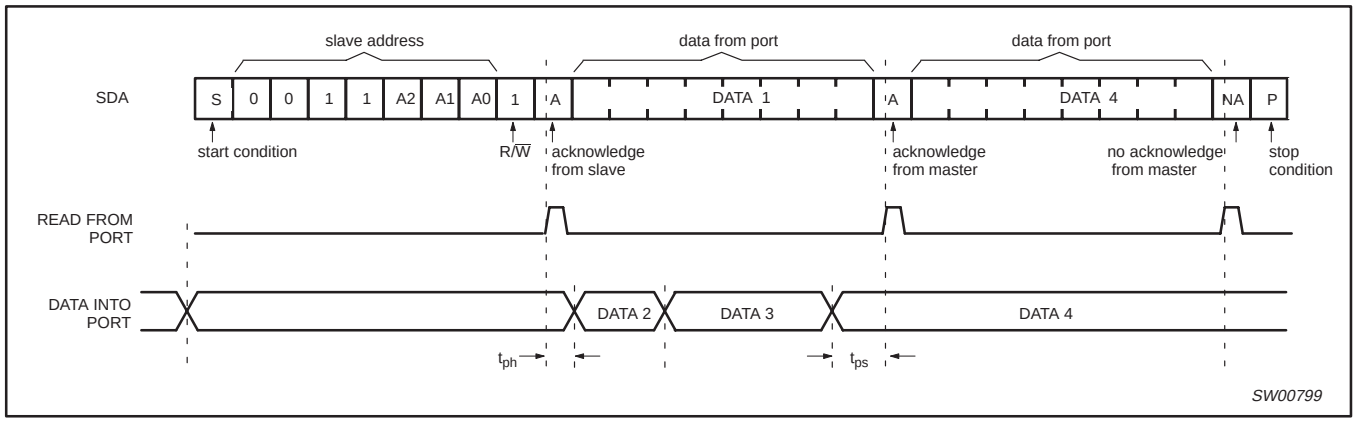


Figure 9. READ from register via Read byte protocol



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.
2. Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Figure 10. READ input port register via Receive byte protocol

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	+6	V
V_I	Input voltage		V_{SS} – 0.5	V_{DD} + 0.5	V
I_I	DC input current		—	± 20	mA
$V_{I/O}$	DC voltage on an I/O as an input other than I/O0		V_{SS} – 0.5	V_{DD} + 0.5	V
$V_{I/O0}$	DC voltage on I/O0 as an input		V_{SS} – 0.5	4.6	V
$I_{I/O0}$	DC input current on I/O0		—	+400	μA
			—	–20	mA
$I_{I/O}$	DC output current on an I/O		—	± 20	mA
P_{tot}	Total power dissipation		—	—	mW
P_O	Power dissipation per output		—	—	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 3.0 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

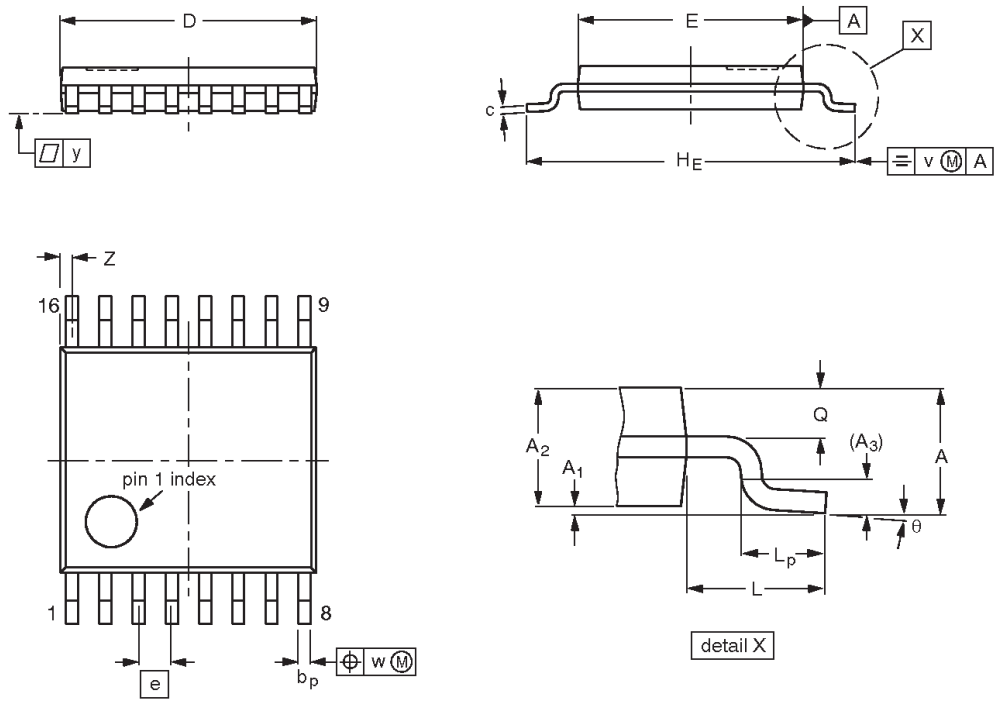
SYMBOL	PARAMETER	CONDITIONS	V_{DD} = 3.3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Supplies									
V_{DD}	Supply voltage		3.0	—	3.6	4.5	—	5.5	V
I_{DD}	Supply current	Operating mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	300	425	—	1100	1500	µA
I_{stb}	Standby current	Standby mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz	—	25	50	–	65	100	µA
V_{POR}	Power-on reset voltage	V_{DD} = 3.3 V; no load; $V_I = V_{DD}$ or V_{SS}; note 1	—	1.3	2.4	–	1.3	2.4	V
Input SCL; input/output SDA									
V_{IL}	LOW level input voltage		–0.5	—	0.8	–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.1	—	5.5	2.1	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	3	—	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	—	10	—	—	10	pF
I/Os									
V_{IL}	LOW level input voltage		–0.5	—	0.8	–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	V_{DD} + 0.5	2.0	—	V_{DD} + 0.5	V
$I_{IHL(max)}$	Maximum allowed input current through protection diode (I/O1 – I/O7)	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	—	—	±400	—	—	±400	µA
I_{OL}	LOW level output current	V_{OL} = 0.55 V; V_{DD} = 3.3 V; note 2	8	10	—	8	10	—	mA
I_{OH}	HIGH level output current except I/O0	V_{OH} = 2.4 V; V_{DD} = 3.3 V; note 3	4	—	—	4	—	—	mA
	HIGH level output current on I/O0	V_{DD} = 3.6 V; V_{OH} = 4.6 V	—	—	1	—	—	1	µA
		V_{DD} = 0 V; V_{OH} = 3.3 V	—	—	1	—	—	1	
I_L	Input leakage current	V_{DD} = 3.6 V; V_I = 0 or V_{DD}	–1	—	1	–1	—	1	µA
C_I	Input capacitance		—	—	10	—	—	10	pF
C_O	Output capacitance		—	—	10	—	—	10	pF
Select Inputs A0, A1, A2, and RESET									
V_{IL}	LOW level input voltage		–0.5	—	0.8	–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	V_{DD} + 0.5	2.0	—	V_{DD} + 0.5	V
I_{LI}	Input leakage current		–1	—	1	–1	—	1	µA

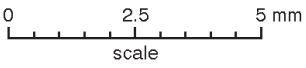
NOTES:
1. The power-on reset circuit resets the SMBus logic with $V_{DD} < V_{POR}$ and sets all I/Os to their default values.
2. The maximum total sink current must be limited to 54 mA at +85 °C, and 80 mA at +70 °C.
3. The maximum total source current must be limited to 54 mA at +85 °C, and 80 mA at +70 °C.

AC SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS		UNITS
		MIN	MAX	
f_{SBM}	SMB operating frequency	10	100	KHz
t_{BUF}	Bus free time between stop and start conditions	4.7	—	µs
$t_{HO:STA}$	Hold time after (repeated) start condition	4.0	—	µs
$t_{SU:STA}$	Repeated start condition setup time	4.7	—	µs
$t_{HO:DAT}$	Data hold time	300	—	ns
$t_{SU:DAT}$	Data setup time	250	—	ns
t_{LOW}	Clock LOW period	4.7	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	µs
t_F	Clock/Data fall time	—	300	ns
t_R	Clock/Data rise time	—	1000	ns
Port Timing				
t_{PV}	Output data valid	—	4	µs
t_{PS}	Input data setup time	0	—	µs
t_{PH}	Input data hold time	4	—	µs
Reset				
t_W	Reset pulse width	2	—	ns

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

Octal SMBus and I²C registered interface PCA9556

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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